VESA® **PLUG and DISPLAY STANDARD**

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VESA PLUG and DISPLAY (P&D ™) STANDARD

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Purpose

This standard is intended to provide an industry standard digital interface for display devices.

Summary

This standard defines a new video interface which provides both digital and analogue interfaces for video data, together with serial bus options.

VESA - The Video Electronics Standards Association
Plug and Display Standard

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B Russell	Canon
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S Slinker	Silicon Image
O Tomita	Toshiba
W Uenishi	Hosiden
H van der Ven	Panasonic
N Vidovich	Hitachi
R Visser	Philips MM Centre

Terms and Abbreviations

Term / Abbreviation	Description
ASIC	Application Specific Integrated Circuit
CRT	Cathode Ray Tube
DDC	(VESA) Display Data Channel
DDC1	The simplest mode defined in the VESA DDC standard
DDC2	The general term used to refer to any of the DDC2 modes (DDC2B, DDC2B+ and DDC2AB) defined in the VESA DDC standard
DDC2B	Simplest of the DDC2 modes defined in VESA DDC standard
DDC2B+	Adds bi-directional communications to DDC2B
DDC2AB	An ACCESS.bus mode defined in VESA DDC standard
DPMS	(VESA) Display Power Management Standard
DSTN-LCD	Dual Scan Super Twisted Nematic LCD
EDID	(VESA) Extended Display Identification Data
EMI	Electromagnetic Interference
EVC	(VESA) Enhanced Video Connector
TFT-LCD	Thin Film Transistor LCD
FPD	Flat Panel Display
FPDI	(VESA) Flat Panel display Interface
HDTV	High Definition Television
IEEE 1394	Standard for High Performance Serial Bus
IC	Integrated Circuit
I^2C™	Trademark of Philips used to refer to the Inter IC or I^2C - Bus
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signaling[1]
Logical Layer	Used to indicate a section of code
MCS	(VESA) Monitor Command Set
Microcross™	Trademark of Molex Inc. for the quasi-coaxial section of the P&D connector system.
P&D™	Trademark of VESA for the Plug and Display standard
PanelLink™ Technology	Trademark of Silicon Image for their LVDS technology
PLL	Phase Lock Loop
Physical Layer	Used to indicate a physical layer, either electrical or mechanical
RFI	Radio Frequency Interference
RGB2S	Red, Green & Blue Video, Hz. and Vt. Syncs.
Rxn	TMDS Receiver number ‘n’
TMDS™ [2]	Trademark of Silicon Image used to refer to their PanelLink Technology[2]
TTL	Transistor, Transistor Logic
Txn	TMDS Transmitter number ‘n’
USB	Universal Serial Bus
VESA	Video Electronics Standards Association

[1] The term LVDS is used in this document as a generic term and does not imply any particular LVDS technology.

[2] The term TMDS will generally be used in this document to denote PanelLink™ or compatible technologies.

Referenced Standards and Documents

Several Standards (listed in following table) are referenced by the P&D standard and compliance with the VESA P&D standard requires compliance with these standards.

Standard Name	Version / Reference	Date
ANSI/EIA-364--1994, Electrical Connector /Socket Test Procedures Including Environmental Classifications	C	Nov. ‘94
ACCESS.bus Specification	3.0	Sep. ‘95
ASME Y14.5M-1994		Jan. ‘95
EIA-170, Electrical Performance Standards - Monochrome Television Studio Facilities - (formerly RS-170)		Nov. ‘57
EIA-343-A, Electrical Performance Standard for High Resolution Monochrome Closed Circuit Television Camera		Sep. ‘69
IEC 801-1, Electromagnetic compatibility for industrial-process measurement and control equipment. Part 1 - General introduction	1984-11	
IEEE-1394-1995	1994	Dec. ‘95
Universal Serial Bus Specification	1.0	Jan. ‘96
Universal Serial Bus Monitor Control Class Definition	0.9g	Nov. ‘96
VESA Display Data Channel Standard	2.01	Apr. ‘96
VESA Display Power Management Signaling Standard	1.0	Aug. ‘93
VESA Enhanced Video Connector Physical Connector Standard	1.0	Feb. '96
VESA Enhanced Video Connector Standard	1.0	Nov. ‘95
VESA Enhanced Video Connector Standard : Proposed Revision	1.2p	Mar. '97
VESA Extended Display Identification Data Standard	2.0	Apr. ‘96
VESA Flat Panel Display Interface 2 Standard Proposal	0.8	Jan. ‘97
VESA Monitor Command Set Proposal	0.2p	Feb. ‘97
VESA Plug and Display Architecture Document [1]	0.1p	Aug. ‘96

[1] Access to the VESA Plug and Display Architecture Document is restricted to VESA member companies.

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1. Introduction

1.1 P&D Overview

The purpose of this standard is to provide a digital interface and, optionally, an analogue interface for video data allowing a wide range of display devices to be attached to a single video port on the host system which may be a personal computer (PC), workstation or other device. This standard only defines the interface at the connector on the host system and provides additional recommendations regarding system implementation.

Monitors using a digital video interface generally have a fixed pixel format, typified by, but not restricted to, a Liquid Crystal Display (LCD) monitor. The objective is to retain data in a digital format thus eliminating the analogue conversion losses that cause screen artifacts. Retaining data in a digital format additionally provides opportunities for reducing system cost and simplifying the display setup.

The digital interface defined in this standard is referred to as Transition Minimised Differential Signaling (TMDS).

Analogue interface monitors are typified by, but not restricted to, CRT (cathode ray tube) based displays.

Prior to the P&D standard, the attachment of digital interface displays to PC's or workstations has required either:

- Conversion of the analogue interface to digital at the display with cost and image quality problems
- Provision of a separate graphics card with a digital interface with cost, space (slot for card), and the issues of a proprietary interface needing to be handled

Key features and benefits of the VESA P&D interface are:

- Single connector for any display device.
- Industry standard, interoperability from multiple suppliers.
- High quality display output.
- Scaleable cost and performance.
- Interoperable solution for analogue and digital monitors.
- Independent software and hardware layers.
- Operating System independent.
- Plug and Play enabled.
- Capable of using existing technology.
- Capable of working over several metres of cable.
- No DC component on interface.
- Low electromagnetic emission.
- Reduced pin count relative to parallel interface (typically 7:1 ratio).

The host receptacle interface defined in this standard is referred to as the P&D-A/D (Plug and Display - Analogue / Digital) in Section 12 which explains the relationships between this and other receptacles in the same family together with the expected monitor plugs.
The P&D-D receptacle shown in Section 12 is a logical extension of this standard for host applications not requiring an analogue option.

1.2 P&D Interface

The term ‘logical layer’ is used in this section to indicate a section of code.

1.2.1 Interface Elements

Feature	Comment
Digital Interface	Mandatory
Analogue Interface[1]	Optional
DDC2	Mandatory
USB	Optional
IEEE 1394-1995	Optional
Initialisation Logical Layer	Mandatory
Command Logical Layer	Optional
Adapter Logical Layer	Mandatory

Table 1-1 : P&D Interface Features

[1] The analogue interface may be either:

- Red, green and blue video with Vsync. and Hsync., or
- Red, green and blue video with composite sync.

1.2.2 Digital Interface: Capabilities

See Section 6 for details of performance ranges, table 1.2 shows the maximum performance capability and the minimum set of features present.

Maximum clock rate	112 MHz	160 MHz (target)
Maximum addressibility	1280 x 1024	1600 x 1280
Maximum refresh rate	60 Hz	60 Hz
Maximum colour capability	24 bpp	24 bpp
DDC2	Yes	Yes
Initialisation layer	Yes	Yes
Adapter logical layer	Yes	Yes

Table 1-2 : P&D Digital Interface Capabilities

Note: The above data rates can be achieved with a 10m cable also but it may not be possible to support either the USB or IEEE-1394 options at >5m, (see their specification documents for details).

1.2.3 Analogue Interface: Capabilities

Ability to support a minimum of 150MHz pixel clock.

1.3 Compatibility with Other VESA Standards

1.3.1 Compatibility with VESA DDC Standard (see Section 2.1)

The VESA P&D standard utilises the VESA DDC Interface to allow configuration data to be sent from the display to graphics subsystem.

The DDC1 protocol is not supported in P&D, but P&D is fully compatible with the DDC2 protocols.

1.3.2 Compatibility with VESA EDID Standard (see Section 2.1)

The VESA P&D standard utilises a configuration data structure defined in VESA Extended Display Identification Data Standard Version 3.

The VESA EDID standard should be read for details of the revised data structure required for the P&D standard.

1.3.3 Compatibility with VESA EVC Standard

The VESA EVC standard provides a high bandwidth analogue video interface, optional serial interfaces, and provision for analogue audio in/out and video in signals.

The VESA P&D standard provides a digital video interface and optional serial interfaces together with the same high bandwidth analogue video interface as EVC.

The VESA EVC and P&D standards share a common connector contact layout but with a different shell giving protection against mis-plugging of monitor and host. See Appendix C, Section 12 for details of plugging options.

Signals that are common to both standards include:

- Analogue video (Red, Green and Blue)
- Horizontal sync.
- Vertical sync.
- DDC bus
- USB bus
- IEEE 1394 bus
- Pixel clock
- Stereo sync.
- Charging power

All of these signals are carried on the same pins in both standards except for the charging power signals, ‘Charge power +’ and ‘Charge power return’. Changes to the EVC standard to match the P&D standard are contained in the EVC Proposed Revision document prepared by the VESA monitor committee.

1.3.3.1 Charging Power

In EVC standard Version 1, charge power is defined as a floating supply. Changing to a ground referenced supply is under review by the VESA Monitor committee.

The VESA P&D standard does not support the analogue audio in and out and video in signals permitted in the EVC standard since these pins have been re-allocated to the digital interface signals.

1.3.3.2 Video Compatibility

The following table addresses video compatibility (see Appendix C, Section 12 for additional details):

System Unit	Monitor	Video Result	Comment on Video Compatibility
EVC	EVC	OK	
EVC	P&D- D	Impossible	Incompatible Plug & Receptacle
P&D-A/D	EVC	OK	
P&D-A/D	P&D-D	OK	
P&D-D	EVC	Impossible	Incompatible Plug & Receptacle
P&D-D	P&D-D	OK	

Table 1-3 : EVC Video Capability

1.3.4 Compatibility with VESA DPMS Standard

The VESA DPMS standard uses the absence of one or both of the horizontal and vertical synchronisation signals to indicate that the display should enter a power saving mode.

If using the analogue interface within the VESA P&D connector, then Hsync. and Vsync. should be used as usual to implement the DPMS standard.

If using the TMDS interface, then the Hsync. and Vsync. (or their equivalents for flat panel displays) signals are coded and multiplexed for transmission but demultiplexed and decoded by the TMDS receiver. They are then available to implement the DPMS standard.

If transmitting the video data over one of the serial bus options, separate provision must be made, if required, to signal power saving modes via a monitor control function. The VESA Monitor Command Set standard defines command codes to implement power saving functions.

1.3.5 Compatibility with VESA FPDI-2 Standard

The VESA Flat Panel Display Interface-2 (FPDI-2) Standard addresses the connection of integrated flat panel display technologies in products such as notebook PCs.

The P&D and FPDI-2 Standards use the same physical transport layer technology (PanelLink™ Technology[1]) with different connectors and cables.

The TMDS Technology has an adjustable output voltage. The maximum cable length in FPDI-2 is 500mm and the maximum cable length in P&D is 10m. For the same differential voltage swing at the receiver, a lower output voltage is required for FPDI-2 resulting in a reduced power requirement.

Note:
[1] In most cases this standard will use TMDS, Transition Minimised Differential Signaling, to indicate PanelLink™ or compatible technology.

1.4 Compatibility with Monitors Using Other Connectors

1.4.1 Compatibility with Monitors Using 15-pin D-sub Connector

These monitors will almost certainly be using an analogue interface. An adapter cable or connector can be provided which would allow attachment to the analogue section of the VESA P&D interface for virtually all monitors which have DDC capability.

Monitors without DDC capability cannot be connected to the P&D interface.

1.4.2 Compatibility with Monitors Using 13W3 Connector

These monitors will almost certainly be using an analogue interface. Many 13W3 implementations do not include DDC and hence they cannot be compliant with the VESA P&D interface.

Those 13W3 connections that do include DDC permit an adapter cable or connector to be provided which would allow attachment to the analogue section of the VESA P&D interface.

1.4.3 Compatibility with Monitors Using BNC Connectors

These monitors will almost certainly be using an analogue interface. Most BNC implementations do not include DDC and hence they cannot be compliant with the VESA P&D interface.

Those BNC connections that do include DDC permit an adapter cable or connector to be provided which would allow attachment to the analogue section of the VESA P&D interface.

1.5 Incompatible Display and System Interfaces

The display shall give a visible and / or audible warning if there is basic incompatibility between the display requirements and the host system capabilities.

This function shall be triggered by detecting that the display interface is connected by monitoring the presence of the DDC +5VDC, if no displayable video is received within 60s of detecting the +5VDC then the display shall indicate incompatibility.

2. Plug and Display Architectural Overview

The P&D architecture is designed as an integrated graphics subsystem with a layered system design concept. The two main layers are logical (software) and physical (electrical and connector).

2.1 Plug and Display System Overview

The Plug and Display Standard is consistent with the VESA Plug and Display Architecture concepts. This architecture is designed to maximise interconnectability whilst allowing many degrees of freedom in choice of the particular interface(s) supported by a particular implementation.

There are two major layers:

- **Logical Layer**
  - The Logical layer is a software layer with multiple sublayers, the Initialisation layer, the Command layer and the Adapter layer. A logical sublayer can communicate with more than one physical sublayer (Interface).
  - The logical layer structure permits independence from a specific operating system and hardware implementation.
  - The following logical layers are mandatory, the Initialisation layer and the Adapter layer.
- **Physical Layer**
  - Within the physical layer optional communications sublayers (or interfaces) may be selected. More than one communications channel is permitted within the Physical Layer.
  - Three sublayers are mandatory:
    - The DDC2 interface to provide configuration data.
    - The TMDS interface for digital video data.
    - The analogue interface for video data

  Other sublayers are optional and may provide such features as control of the display device, attachment of additional devices, etc.

The P&D interface is designed for point to point uni-directional video high speed data communication between a host (e.g. a PC or Workstation) and a Monitor but is also able to support bi-directional multi-port medium speed command, control and data transfer connectivity . The Monitor may be comprised not only of a display transducer but also a wide range of I/O. e.g. Digital Cameras, CD ROMs, Keyboards, Mice, Pointing Devices, Sound I/O.

2.2 P&D Architecture

Reference Section 2.3 for conceptual drawing.

2.2.1 Logical Layer Concepts

The Logical layer comprises of three sublayers:

- **Initialisation Layer**

  This layer is mandatory.
- **Command Layer**
  The command layer provides support for video transducer control and low speed I/O data streams.
- **Adapter Layer**
  The adapter layer provides transport mechanism of video data stream from the application and operating system to the display device.

The **Initialisation Logical Layer** is a mandatory section of code which :

a) Starts and Controls the DDC2 data from the display device to the host and places the DDC2 data into a buffer.
b) Analyses the DDC2 data and configures the communications channel(s) in the system adapter(s) to match the channel resources in the monitor and the I/O attached to the monitor.

This layer of code may function prior to the operating system being loaded or during the loading of the operating system.

The **Command Logical Layer** is an optional layer of code that:

Controls the monitor in terms of setting parameters (e.g. colour temperature) , reading status and running diagnostics.
For those digital monitors which do not support the command layer, power management is controlled using the protocol specified by the VESA DPMS standard.
Either USB or IEEE-1394 may be used as the Command layer.
Low speed I/O devices (keyboard, pointing devices, etc.) may be attached via USB whether it is the Command layer or not.
High speed I/O devices (CDROM, hard disk drive, camera etc.) may be attached IEEE 1394 whether it is the Command layer or not.

The **Adapter Logical Layer** provides:

The interface for the unidirectional high speed video data bus or a high speed bi-directional channel(s) which allows video devices,(in-head display adapters, digital camera) and display adapter in the PC or Workstation.
This layer is mandatory

2.2.2 Physical Layer Concepts

The physical layer comprises two sublayers:

- **Electrical physical layers**
- **Mechanical physical layer**

2.2.2.1 Electrical Physical Layers

The electrical physical sublayers may be either the electrical interface at a physical connector or an electrical interface between two function units on a logic card or within a VLSI Module. The interface defined here is at the connector pins after the output transmitters.

A DDC2B (with +Vcc and GND supplied by the system unit) physical sublayer is mandatory to carry configuration data from the display to the host during host initialisation and operating system load.

Note: DDC2B is the minimum level of performance, an implementor may choose to use DDC2B+ or DDC2AB instead.

The TMDS and DDC2 electrical sublayers are mandatory, other electrical sublayers are optional.

2.2.2.2 Mechanical Physical Layer

This is the layer where the type and pin assignment configuration of the connector is defined. See Section 7 for specification.

Note: Specification of a particular cable type is outside the scope of this standard, however, Section 8 provides guidance on likely performance requirements.

2.2.3 Explanation of Remaining Elements of P&D Architecture Overview Drawing

Reference: Section 2.3

- Graphics Engine

  This section covers the graphics chip, graphic accelerator, etc.

- Frame or Refresh Buffer

  A block of memory used to store and manipulate the displayed image(s).

- Optional Interconnection USB, IEEE 1394, etc.

  This represents the optional serial buses that may be used either to provide video data or to control of the display and / or provide attachment of other devices.

- I^2C Hardware

  The hardware required to support a DDC2B (or DDC2B+ or DDC2AB) interface.

- Host Video Receptacle

  A representation of the physical receptacle on the host system.

- Display Video Cable Plug

  A representation of the physical plug on the host end of the video cable.

- Optional Frame or Refresh Buffer

  An optional frame or refresh buffer which may be required for some technologies or be an alternate design point.

- Display Device

  The actual display device.

2.3 P&D-A/D Connector Overview

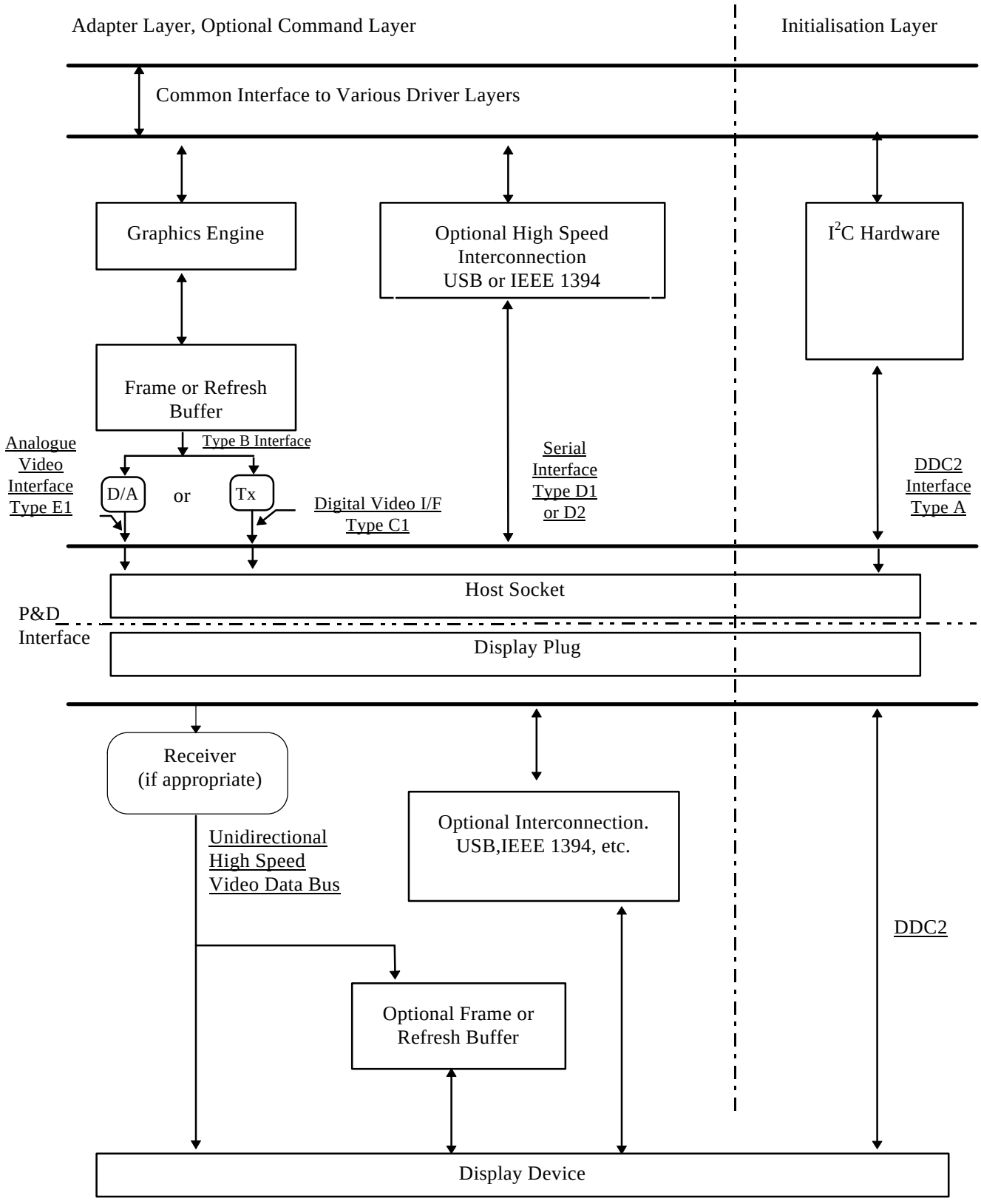


Figure 2-1 : P&D-A/D Connector Overview

3. Detection of Display Disconnect

The VESA Plug and Display Standard supports hot-plugging of the display device. The primary purpose is to protect the display device from possibly dangerous conditions created by receiving data at an inappropriate frequency and/or format. There are elements of the detection mechanism at the host and display ends.

Notes:

1. The flowchart in Section 3.3 and following text assume that monitor design incorporates DPMS.
2. DPMS is optional under P&D.

3.1 Detection Mechanism - Host

Reference the flowchart in section 3.3 which is intended for process illustration only.

Initially the host system shall provide the +5V DDC line and then check to see if an EDID can be read at address A2h. The host should retry this operation for up to 30s.

If no EDID is detected at A2h, then the host shall check for an EDID at A0h. If an EDID is present then the EDID contents should be decoded to provide supported mode information.

If no EDID is present then carry on to check for presence of a colour or monochrome monitor by checking for load on the R/G/B lines, if a monitor is present then assume it has minimum VGA capability.

If an EDID is detected at A2h, if a P&D monitor bit is set in EDID check that the charge power line has ≥ 2.0V from the monitor to indicate that the monitor is ready. **Note: The charge power line may be up to 20V.**

If the EDID requested use of the TMDS interface, then enable the TMDS transmitter.

Continue to monitor the Charge power line for ≥ 2.0V, if the voltage drops then assume the monitor has been unplugged, immediately disable the TMDS transmitter (if it was enabled) and wait until the ≥2.0V signal is re-established indicating that a monitor, the same one or a different one, has been attached. The graphic sub-system should raise an interrupt to the operating system which should cause the operating system to initiate action to reread the EDID and take appropriate action based on the contents of the new EDID.

A status shall be set indicating what monitor capability has been detected (or assumed) and when the TMDS transmitter is enabled or disabled.

3.2 Detection Mechanism - Display

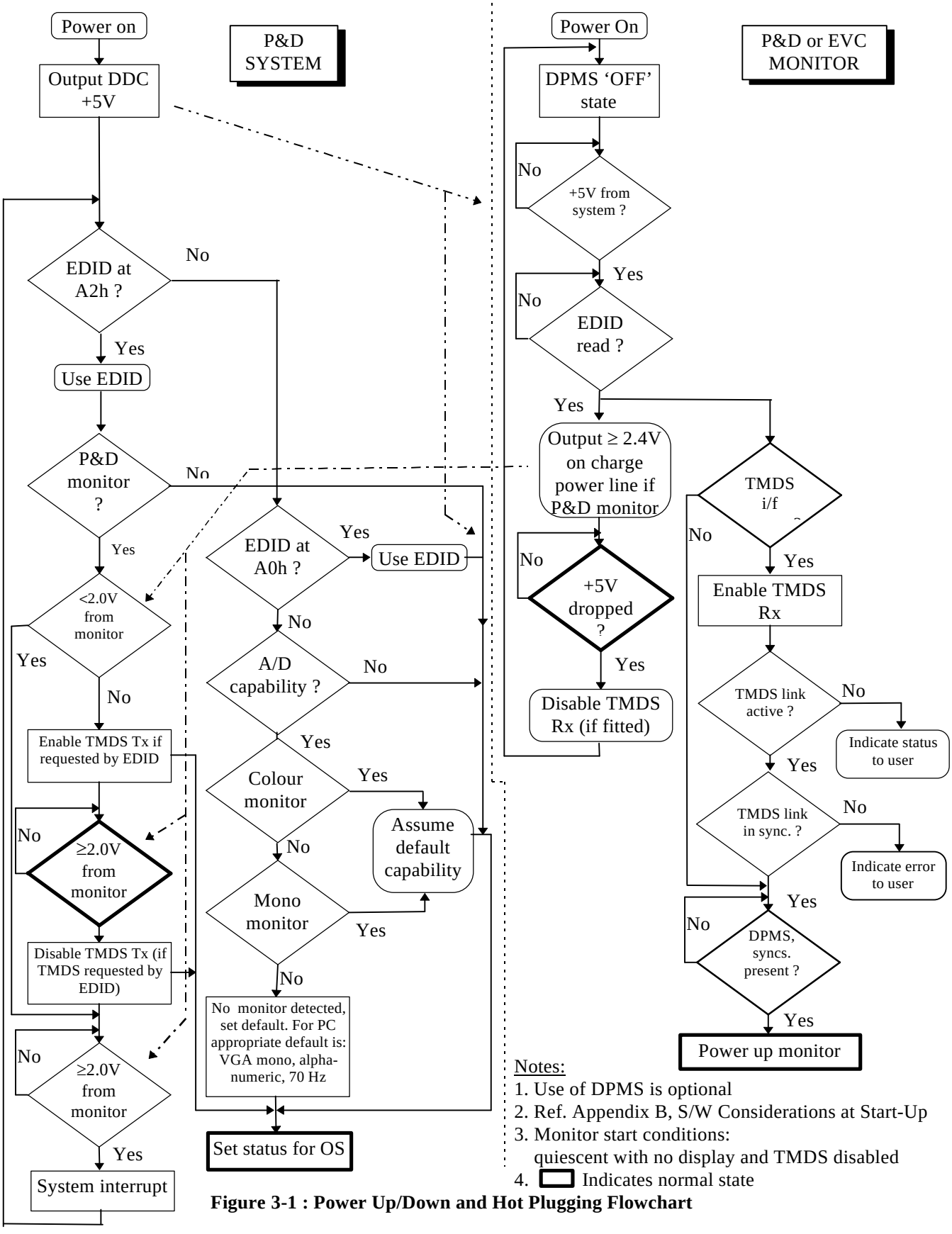
Reference the flowchart in Section 3.3 which is intended for process illustration only.

When power is applied initially the display should be in a quiescent state with no displayed image and the TMDS receiver (if present) disabled. The DDC +5V line from the system shall be monitored, if +5V is present then, assuming monitor power is enabled, output ≥ 2.4V on the Charge Power line if it is a P&D monitor. If a TMDS receiver is present then enable it, then check if the link is active and synchronised. Indicate 'link inactive' and, if necessary, 'link unsynchronised' status to user.

The DPMS circuit will then power up the monitor once the Hz. and Vt. sync. signals are detected.

Continue to monitor the +5V line, if the line drops for to <2.0V for ≥1s after being present for ≥60s then a hot plug condition exists. The display shall disable the TMDS receiver, if fitted, and indicate the status to the user by an appropriate technique e.g. flashing LED, on screen message, etc. After an appropriate period, the display should return to the initial quiescent state.

3.3 Power Up/Down and Hot Plugging : Flowchart



Notes:
1. Use of DPMS is optional
2. Ref. Appendix B, S/W Considerations at Start-Up
3. Monitor start conditions:
   quiescent with no display and TMDS disabled
4. ▭ Indicates normal state

Figure 3-1 : Power Up/Down and Hot Plugging Flowchart

4. Electrical Layer Specification: Part 1

The Electrical Layer Specification has been split into 3 sections. This section deals with all aspects except for the TMDS interface and Section 6 gives the detailed specification of the TMDS interface at the P&D connector. Section 5 is inserted to give an overview of the TMDS interface technology, it is not considered to be part of this standard.

4.1 Introduction

Each sublayer is identified by its function and also a designation of "Type x" where 'x' represents a variety of possible alphanumeric codes. These type codes are a cross-reference to the VESA P&D Architecture Document.

Type Designation	Corresponding Sublayer
A	DDC2
C1	TMDS Interface[1]
D1	IEEE 1394-1995
D2	USB
E1	EDID Defined Analogue

Table 4-1 : Electric Sublayers

[1] The TMDS Interface is considered in Sections 5 and 6.

4.2 DDC2 Sublayer, Type A

The DDC2 sublayer interface is a simple low cost serial interface for the initialisation of the P&D. DDC2B is the minimum level required to comply with this standard, DDC2B+ or DDC2AB may, optionally, be used for control of the monitor. This a mandatory electrical sublayer.

DDC2B is a point to point bi-directional channel between the display and the host system, the VESA Display Data Channel Standard contains the full definition.

4.2.1 List of Signals

Signal Name	I^2C Bus Name
DDC Data	SDL
DDC Clock	SCL
+5V DC	
DDC Return	

Table 4-2 : DDC2 Sublayer Signals

4.2.2 Signal Specification and Timing

The VESA DDC Standard Version 2 contains definitions of signal specifications and timing.

4.2.3 Extended Display identification Data (EDID)

The VESA EDID Version 3 standard contains a specific data format for use with this P&D Standard.

4.3 IEEE 1394-1995 Sublayer, Type D1

See IEEE 1394-1995 (High Speed Bus) Specification for details.

4.4 USB Sublayer, Type D2

See Universal Bus Specification for details.

4.5 Analogue Sublayer, Type E1

The analogue sublayer has a number of options (e.g. signal amplitude and polarity). The EDID transmitted by the display will define the option(s) to be used.

4.5.1 Analogue Interface

As a method of supporting the current variable format analogue monitors, a RGB with line sync. and frame sync. sublayer interface is supported.

4.5.1.1 List of Signals

Signal	Signal Level
Red Video Out	See Section 4.5.2
Green Video Out	See Section 4.5.2
Blue Video Out	See Section 4.5.2
Pixel Clock Out (optional)	See Section 4.5.4
Video Return	
Hz. Sync. Out	See Section 4.5.3
Vt. Sync. Out	See Section 4.5.3
Sync. Return	
Stereo Sync.	See Section 4.7

Table 4-1 : Analogue Sublayer Signals

4.5.2 Analogue Video Signals

The video signals provided by the P&D shall comply with the following requirements. Please note that this standard includes the new VESA video signal standard originally introduced in the VESA EVC standard which may be used if desired. Systems may continue to use the earlier signal standards while using the P&D, as long as support for the appropriate standard is identified by the display in the EDID information, and if the overall requirements for those signals under P&D are met.

4.5.2.1 Signal Amplitude and Polarity

All video signals provided by systems using the P&D shall be interpreted such that increasingly positive voltages in excess of the defined black level correspond to increasing luminance in the displayed image.
i.e. the P&D shall always provide "white-positive" video signals.

The signal amplitude standard expected by the display will be provided by that display via its EDID but must conform to one of the following standards:

	Type 1 "RS-170"[1]	**Type 2 "RS-343"[1]**	**Type 3 "Euro"**	**Type 4 VESA**
White (peak)[2]	+ 1.000 V	+ 0.714 V	+ 0.700 V	+ 0.700 VDC
Black[3]	+ 0.075 V	+ 0.054 V	+ 0.000 V	+ 0.000 VDC
Blank	Reference	Reference	Reference	+ 0.000 VDC
Sync. tip[4]	- 0.400 V	- 0.286 V	- 0.300 V	None

Table 4-2 : Video Signal Amplitude and Polarity

[1] - The terms "RS-170" and "RS-343" properly refer to two classes of former standards which were established by the Electronic Industries Association (EIA). As these terms have been commonly used within the computer display industry, they refer only to the signal level standards listed above. Refer to the EIA standards for full definition of these signals.

[2] - White is defined as the peak signal level, excluding overshoot, ringing, noise, and similar transients, which is transmitted during the active video time i.e. that period of the video signal exclusive of the blanking time.

[3] - Black is defined as the minimum signal level expected during the active video time. The RS-170 and RS-343 standards define a difference between "black" and "blank", known as the "setup". Setup may be considered optional under these standards, but the display should communicate (via the EDID) whether or not setup is expected.

[4] -The sync. tip level refers to the signal amplitude defined for the case of sync-on-video. In systems providing sync-on-video, this information should appear only on the Green video signal except in the case where the Red, Green and Blue signal outputs are being used to provide simultaneous monochrome outputs. Sync. information shall not be provided on any video signal output when separate sync. signals are in use. Sync-on-video may not be used when operating under the VESA video signal standard.

4.5.2.2 Reference level

With the exception of the VESA video signal standard, the above listed standards are intended for AC-coupled video inputs and use the blank level as the signal reference. The VESA video signal standard is intended for DC-coupled systems, and the reference point under this standard is the signal common as established by the return for the video signals (pin C5 of P&D-A/D).

4.5.2.3 System Impedance

Any analogue video output driver, display input, cabling, etc., used in a P&D-A/D based system shall be designed assuming a nominal impedance of 75Ω for the analogue video signal transmission system.

4.5.3 Synchronisation Signals - VESA Video Signal Standard

Except as noted below, the following requirements shall apply to those systems employing the P&D-A/D and using the VESA video signal standard.

4.5.3.1 Combining Synchronisation and Video (Luminance) Signals

Video systems using the VESA video signal standard shall not supply or use synchronisation pulses combined with the luminance signals defined above. i.e. there shall be no sync-on-green or equivalent.

Synchronisation signals shall always be supplied to the display by means of separate, dedicated signal lines.

4.5.3.2 Sync Signals Under the VESA Video Standard

Horizontal sync. pulses shall at all times continue to be supplied during the vertical sync. pulse period. Under the VESA video signal standard, use of composite sync. on either separate sync. line is not permitted.

4.5.3.3 Synchronisation Signal levels and Tolerances

It is expected that the synchronisation signals will be communicated using one or more standard logic family levels, and that strictly defining the expected signal levels for all cases is therefore beyond the scope of this standard. However, the following standards should be recognised for the specific cases of the TTL families.

Logic Family	TTL (all families)
Logic “1” level	min. 2.4 V (driver), 2.0 V (receiver)
Logic “0” level	max. 0.5 V (driver), 0.8 V (receiver)
Rise / Fall time	< 10 ns (20 - 80%)

Table 4-3 : Synchronisation Signal Specification

4.5.3.4 Termination of Synchronisation Signal Lines; Loading

In the case of systems using the TTL logic levels as defined above, the standard termination presented on the synchronisation lines by the display device shall be a nominal 2 KΩ to +5 VDC.

4.5.4 Pixel Clock

The P&D receptacle provides for an optional Pixel Clock, intended for use by flat-panel based displays or similar systems which require a clock to sample the video output signals. This pixel clock is not required to be present on the P&D unless some level of flat-panel support via the analogue interface portion is intended, and may be enabled or disabled by the host depending on whether or not the display in question requests it via the display’s EDID.

When provided the clock output shall meet the following requirements, as measured at the P&D output pin and using a standard (75Ω +/- 1%) resistive termination connected as closely as possible to that point.

4.5.4.1 Signal Amplitude and Offset

The clock signal amplitude shall be 0.7 Vp-p, +/- 0.1 V. The signal shall have 0.0V DC offset, meaning that the logical “0” portions of the signal shall be at 0.0V DC (as defined by the signal ground, pin C5), with the logical “1” state at a nominal + 0.7V from this reference.

4.5.4.2 System Impedance

75Ω nominal.

4.5.4.3 Active Edge

It shall be standard that the active edge of the pixel clock (the edge on which the video is expected to be sampled) shall be the rising edge i.e. the positive going transition.

4.5.4.4 Skew

The skew of the pixel clock shall be controlled such that the 50% point of the rising edge occurs at the midpoint (50%) of the pixel period within the green video signal +/- 90 degrees.

4.5.4.5 Rise / Fall Time

The rise time (positive going transition) of the pixel clock signal, as measured between the 10% and 90% points, shall not be greater than 20% of the pixel period of the fastest pixel clock supported in this mode of operation. There is no specific requirement on the clock fall time, other than it be sufficiently short so as to permit a low (logical “0”) time (signal at or below 0.1 V) of not less than 35% of the clock period.

4.5.4.6 Overshoot / Undershoot, Ringing

The overshoot, undershoot, and ringing of the pixel clock signal shall be controlled so that no portion of the clock signal falls outside of the range +/- 0.15V of the nominal amplitude for the high or low state following the rising or falling transition, respectively.

The above requirements are summarised in the following diagram:

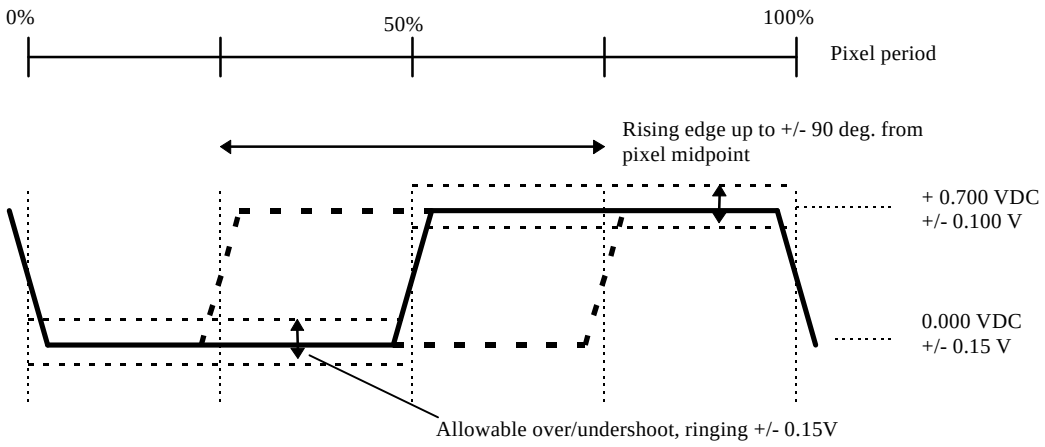


Figure 4-4 : Stereo Sync.

4.6 Charging Power

The charging power input is used by the host computer (typically a notebook or similar portable computer) as a source of charging power for its internal batteries (if fitted). **Support for this input is optional and a host with no need for charging power is not required to provide any connection or load on this line except for the hot plugging scheme requirements specified in Section 2**. Display devices intended for connection to a host may provide charging power on this pin as desired.

The following restrictions apply:

1. **Charging Voltage**
   18 → 20 VDC.

2. **Current**
   Maximum of 1.5A in normal "full-on" state. The current available on this pin shall at all times be limited to not more than this value long term, and not more than 5A for not more than 2s. The device supplying the power must be designed so that no damage or safety hazard occurs under any load condition, including a short or ground applied for an indefinite period.

3. **Current Control, Default State, and Loss of Connection**
   The charging current shall at all times be under the control of the host device (the device being charged).
   The default (power up) state for the charging supply shall be the trickle charge state, as described below.
   The charging supply shall be switched to the "full on" state described above only upon detection of a host connection via sensing of the +5 VDC supply on pin # 8 (any time the voltage present on this line exceeds +2.0 VDC for a continuous period of not less than 10 μs), or under the command of the host device.
   The charging supply shall also be designed to return to the trickle charge state within 10ms of disconnection from the host, identified by loss of the +5 VDC supply (pin # 8) from the host (any time the voltage on this line is less than 0.8 VDC for a continuous period of not less than 10 μs).

4. **Trickle Charge Current Limit**
   In the "trickle charge" state, entered either under host control via a monitor command or upon disconnection from the host as described above, the charging current must not exceed 50mA under any load condition.

5. **Command Set**
   The commands used to control the various states of the charging power connection are defined in the VESA Monitor Command Set and may be carried by either:
   - The ACCESS.bus specification
   - The USB Video Class Device Specification

4.6.1 Hot Plugging

When used for hot plugging protection only, the voltage output on the charging power line must be ≥2.4V at a maximum of 50mA (under any conditions) as measured at the video cable plug.

4.7 Stereo Syncronisation

A signal for the syncronisation of stereoscopic displays may optionally be provided on the P&D pin # 24. This signal shall meet the level, termination, and loading requirements as listed in Section 4.5.3, and shall be subject to the following additional requirements:

If using the TMDS portion of the P&D interface then the stereo sync. signal, if required, shall be connected to the CLT3 input of the TMDS transmitter.

1. The stereo sync. signal shall be a nominal 50% duty cycle square wave at one-half the vertical sync. rate currently in use. The transitions of the stereo sync. signal shall take place within three horizontal line times of the start of the vertical blanking period, but in no case shall the stereo sync. transition occur prior to the start of vertical blanking.

2. Unless otherwise specified by the EDID, the sense of the stereo sync. signal shall be that the signal is high (logical “1” level) during that period corresponding to the left eye field, and low during the right eye field. An idle line in either state (the line may be considered idle if more than 3 vertical sync. pulses occur with no transition on the stereo sync. line) shall be interpreted as meaning that the stereoscopic display is no longer in use (the image being displayed is in the normal “flat” mode).

5. Electrical Layer Specification: Digital (TMDS) Video Transmission Overview

Note: This section is an overview of the TMDS Interface and includes elements which are not part of the P&D standard.

5.1 Transition Minimised Differential Signaling Interface Overview

The VESA FPDI-2 and P&D Transition Minimised Differential Signaling (TMDS), interface standard is based on PanelLink™ Technology developed by Silicon Image, Inc. of Palo Alto, California. The TMDS interface takes parallel data from the host graphics controller and transmits it serially at high speed to the receiver.

The characteristics of this interface are:

- Uses 3 differential data pairs with timing and control data embedded in data transmission.
- Uses transition controlled binary DC balanced coding for reliable, low-power, and high-speed data transmission.
- Uses low-swing differential voltage.

5.1.1 Introduction

As the data rate from a variety of multimedia sources is increasing at the desktop computing systems interface, a safe and reliable transmission of data at high-speed essential. Video data transmission between computer systems and flat-panel displays (e.g. liquid crystal displays) requires higher speed interconnects for increasing video data. Existing digital interconnect systems for such applications typically employ single ended parallel data streams. The bandwidth requirement increases following the increase in display addressibility or allowing multiple devices to be connected and the parallel interface may give problems with EMI and noisy transmission.

The number of signals required in a parallel interface makes the video transmission difficult and inflexible as signals may interfere each other and thus cables are short. The TMDS interconnect system not only reduces the number of data signals required for high bandwidth data transmission but also minimises the EMI using low swing differential voltage transmission with a new coding scheme for low power operation and simple clocking methods. TMDS technology uses a DC balanced and transition minimised coding scheme for low power operation, and a method of embedding timing and video control signals into the data streams, which further reduces the number of signals required. TMDS technology can be applied to interfacing LCDs and other flat-panel displays that require digital interface for reliable data transmission or remote display application where distance between the display and the host system is relatively long. In the latter case, the transmission media can be fiber optics using serial digital signal.

5.1.2 Logical Architecture

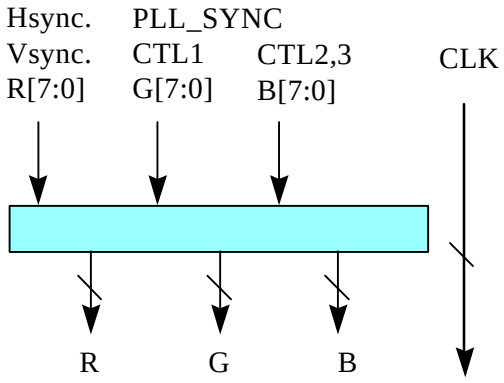


Figure 5-1 : Simplified Block Diagram of a TMDS Interface with Clock + RGB

The high-data rate link system is composed of 3 data lines and an accompanying clock. Signal transmission media can be either a terminated cables such as twin-axial cable or twisted pair with screen return or an optical fiber, in this case a driver and an amplifier for a laser diode and a PIN diode respectively are a signal load and a source for the video link.
The voltage swing on the cable is adjustable[1] with 500mV being the recommended voltage. Since its swing is differential on the pair, the net signal on the pair is required to have a swing twice larger than the single-ended signal. It is required to make the transmitter interface have an externally adjustable current level, in cases when a standard level is not used for maximal current reduction. The implemented interconnect system is required to use low-swing signal on only four terminated lines, so there will be significantly reduced electromagnetic interference (EMI).

For an unconditionally P&D TMDS inter-operable transmitter, the output current level is set at the maximum (12 mA). For limited-domain applications (e.g. notebooks) make the output current level adjustable so that the transmitter can accommodate various kinds of cable and receiver types with minimum power.

The voltage difference between the AVCC and EXT_SWING pin determines the voltage swing of the differential signal pairs. This adjustable low voltage differential swing can be used for various cable lengths. A larger voltage swing would be used for longer cables, and a lower voltage swing should be used for shorter cables. Sometimes larger voltage swings can cause noise on shorter cables due to transmission line effects. It is absolutely necessary to adjust the voltage swing accordingly to the length and type of the cable. The larger the voltage swing, the higher the power consumption.

If the EXT_SWING pin is left unconnected, the internal voltage divider circuit will set the EXT_SWING pin at approximately 2.8V when AVCC is at 3.3V, producing approximately a 500mV swing on the differential signal pairs. The differential voltage level swing for single ended is set by the formula:

$\mathbf{V_{SWING} = 0.5V \times (500\Omega / R_{EXT\_SWING})}$ where V_{SWING} = Single Ended Differential voltage swing

R_{EXT_SWING} = External Resistor on EXT_SWING pin

Rs (RPOT1)	Vs (Theoretical Calculation)
300Ω	833mV
400Ω	625mV
500Ω	500mV
600Ω	417mV
700Ω	357mV
800Ω	313mV
900Ω	278mV
1KΩ	250mV

Table 5-1 : Theoretical Low Voltage Single Ended Differential Swing Level Relative to R_{EXT_SWING}

[1] The P&D standard requires the voltage swing to be preset.

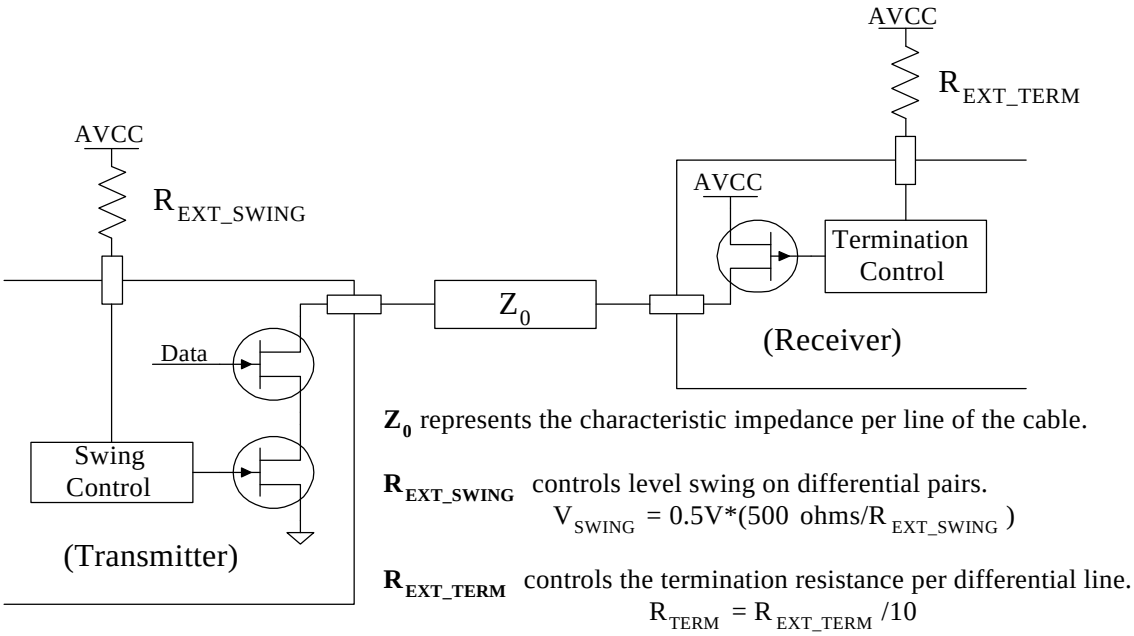


Figure 5-2 : Transition Minimised Differential Voltage Swing Adjust

From the above figure, TMDS technology uses current drive to develop the low voltage differential signal at the receiver side of the transmission line.

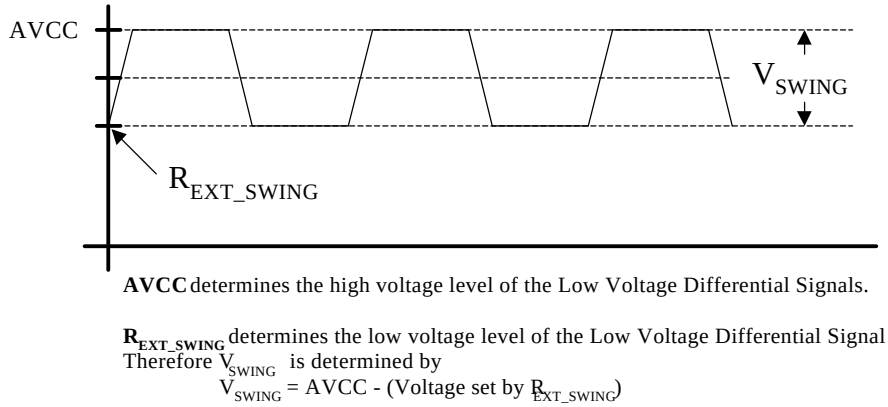
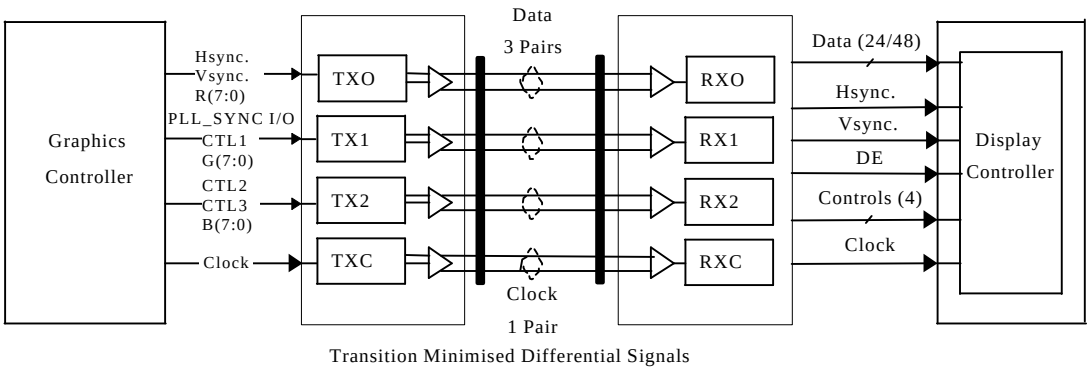


Figure 5-3 : Single Ended Transition Minimised Differential Signal Adjustment

From figure 5.3, the high voltage level of the low voltage differential signals will be set by AVCC, the low voltage is adjustable with the low voltage differential swing control circuit. The low voltage differential voltage swing is adjustable by using a potentiometer (R_{EXT_SWING}).

Video signals are composed of three separate signals, typically RGB, along with two synchronisation signals called Hsync. and Vsync. Instead of having extra lines, those two sync. signals are mixed with the RGB data in the encoder, thereby limiting the number of data pairs to three. The transition-controlled digital encoding will encode 8-bit of data, data enable (DE), and 2-bit of control signals. Control signals are allowed to change only during “blank” time when DE is low/inactive, therefore, the levels of the control signals are constant during active data area when DE is high.



Note: Each pair requires a current return

Figure 5-4 : System Environment Block Diagram Example

The system provides parallel interfaces to both the computer system's display/graphics controller and the display devices, and thus no modification to existing system is required other than adding a TMDS transmitter IC and a TMDS receiver IC.

5.1.3 Summary

TMDS technology implements a high-speed video data transmission system capable of converting parallel video data stream and video display timing and control signals to three high-speed serial differential data pairs at speeds capable of supporting high-resolution displays (e.g. 800x600 color pixels and above addressibilities).

Shown below is a sample of typical monitor requirements for update and refresh rates:

Addressability	Frame Rate (Hz)	Pixel Clock (MHz)	Data Rate (Mbytes/s) Post Palette 12bpp	Data Rate (Mbytes/s) Post Palette 24bpp
Update Rate (Shadow Buffer in Monitor)				
640 x 480	60	25	37.5	75
720 x 400	70	28	42	84
800 x 600	60	40	60	120
1024 x 768	30	23.59	35.38	70.77
1280 x 1024	30	40	60	120
2000 x 2000	30	120	180	360
1280 x 720	30	27.64	41.46	82.92
1920 x 1080	30	62.2	93.3	186.6
CRT Compatible Refresh Rates				
640 x 480	60	25	37.7	75
720 x 400	70	28	42	84
800 x 600	60	40	60	120
1024 x 768	60	65	97.5	195
1280 x 1024	60	112	168	336
1600 x 1200	75	250	375	750
2500 x 2000	75	384	575	1150
1280 x 720	60	77.5	116.25	232.5
1920 x 1080	30(1)	77.5	115.8	231.6

Table 5-2 : Addressability Table

5.1.4 TMDS Transmitter

The transmitter is a serial link sharing a common clock. It accepts parallel data streams and converts them into serial data streams. The clock line does not bear the same frequency as the data rate on the transmission wire. Effective data transmission is 10 times the input clock frequency. One of the advantages of this scheme is power reduction.

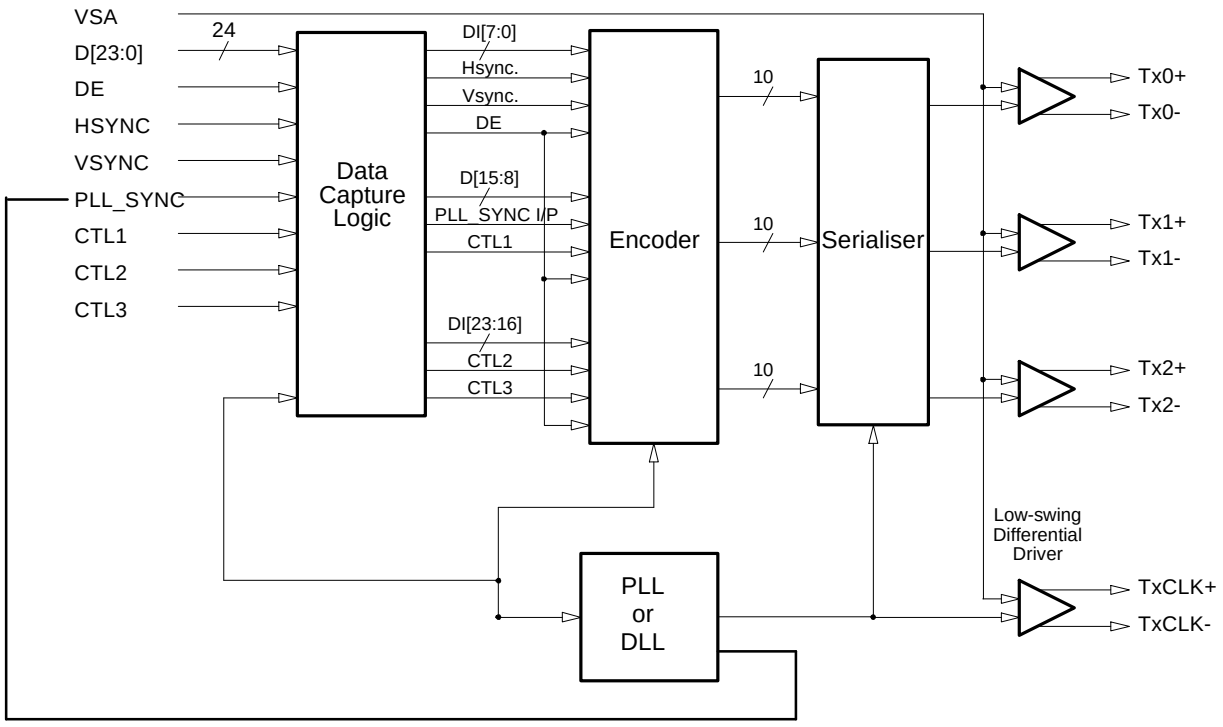


Figure 5-5 : TMDS Transmitter IC Functional Block Diagram

Figure 5.5 shows a TMDS transmitter IC functional block diagram. The transmitter IC consists of a data capture logic block, data encoder block, serialiser block, three high-speed differential data pair and differential clock line drivers. The encoder converts 8 bits of data into 10 bits of transition controlled and DC balanced data stream. The serialiser takes 10-bit encoded data as an input and serialises it according to the differential data pair speed required for the display addressibility. The differential data pair drivers implements adjustable differential voltage swing drivers. These are open drain drivers which requires receiver-end termination with pull-up resistors matching the impedance of the interconnect system, as shown in Figure 5.6.

A TMDS interconnect system is composed of 3 data pairs and an accompanying clock pair with a reduced differential logic swing and with a DC-balanced data stream for transformer or capacitor coupling. Signal transmission media can be either a terminated wires such as twinax cable or twisted pair or an optical fiber, in this case a driver and an amplifier for a laser diode and a PIN diode respectively are a signal load and a source for the video link.

There are two ways to encode the control signals when DE is low. The first method uses edge transitions (rise/fall) of the control signals and the second method uses the levels (high/low) of control signals. TMDS encoding uses the latter, encoding levels of control signals. TMDS's proprietary encoding method guarantees transition-minimised and DC balanced character set for the data. Three special characters are used to encode the control signals. A total of 260 (256 in-band data set and 4 out-of-band special character set) 10-bit characters are required for each encoder as shown in the following table:

Data [7:0]	DE	Control 1	10-bit code
1 to 256	High	-	C_1-C_{256}
-	Low	Low	C_{257}
-	Low	Low	C_{258}
-	Low	High	C_{259}
-	Low	High	C_{260}

Table 5-3 : Encoder Mapping for a Single Differential Data Pair

The encoder generates one of the four kinds of special characters according to the level of Hsync. and Vsync. (or 2 control inputs) when DE is LOW. When DE is high, 8-bit data is converted to 10-bit transition minimised and DC-balanced in-band data.

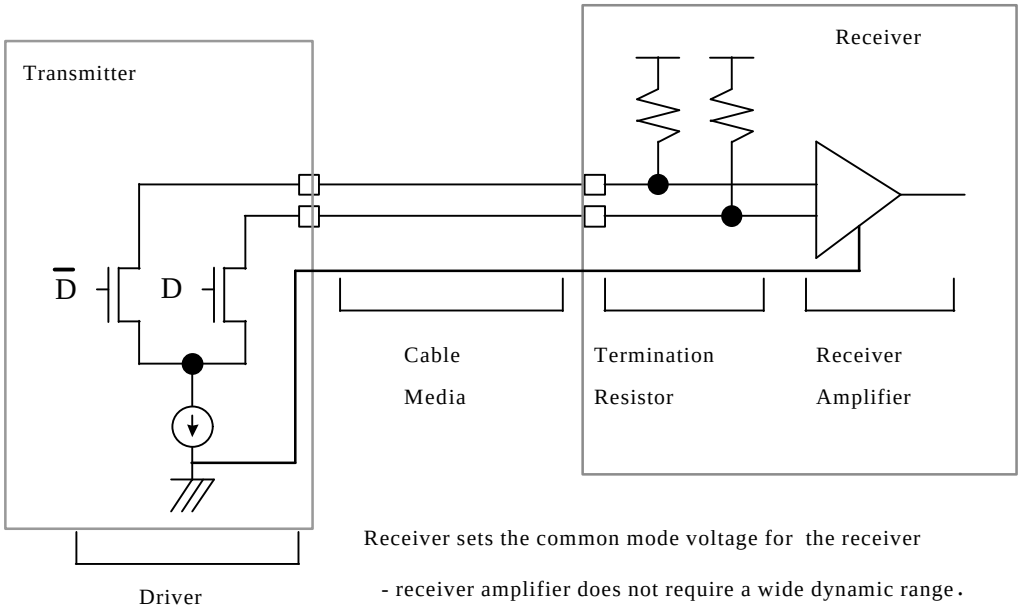


Figure 5-6 : Typical CMOS Circuits for TMDS Driver

The voltage swing on the pair is adjustable but 1V is the typical differential voltage. Since its swing is differential on the pair, the net signal on the pair has a swing twice larger than the single-ended signal. A differential swing of 1V is enough to drive a receiver, it is possible to reduce the voltage swing depending on the quality and length of the wire without reducing performance. Since the voltage on the cable is developed by the current drawn by the receiver, with reduced swing, the power dissipation is reduced. With a larger characteristic impedance on the cable, it is possible to develop the same voltage with reduced amount of current, reducing the power further. The input of the receiver is a differential voltage, the transmitter is two single ended current sinks with the return current via the outer of each pair, either D or $\overline{D}$ conducts the current. It is very important to make the receiver have an externally adjustable current level, when a standard level is not used for maximal current reduction. Since TMDS interconnect systems use a low-swing signal on only four terminated lines, there will be significantly reduced electromagnetic interference(EMI) relative to fully parallel interfaces.

5.1.5 TMDS Receiver Summary

Note: This section is included for completeness but does not constitute part of the P&D standard.

The receiver converts the transmitter's data stream using the differential pixel clock provided with the three serial data streams. Since there is no assumption on the related timing between clock and three data lines, the receiver blindly oversamples the data with the multiphase clocks and digital logic extracts data in later stages in the digital domain. The multiphase clocks are generated in the PLL from the reference clock which is transmitted with the data signals. Since only one datum is selected as an output out of the three sampled data, only one sampler will be activated after correct timing is determined. The remaining two will be deactivated until the next timing adjustment is needed, resulting in power-saving. Since three differential data pairs might have different line length, the correct sampling time will be different from differential data pair to differential data pair. The correct sampling time is individually obtained and the correct word is assembled from the three data streams to form parallel data using the information of intermittent synchronising patterns.

Figure 5.7 shows a TMDS receiver functional block diagram. The TMDS receiver chip consists of three differential receiver circuits, data recovery block, decoder block, and panel interface logic. The host graphics controller may use different clock frequencies for different display modes, therefore the receiver clock should be derived from the clock transmitted by the transmitter chip which goes to the RxCLK+ and RxCLK- pins.

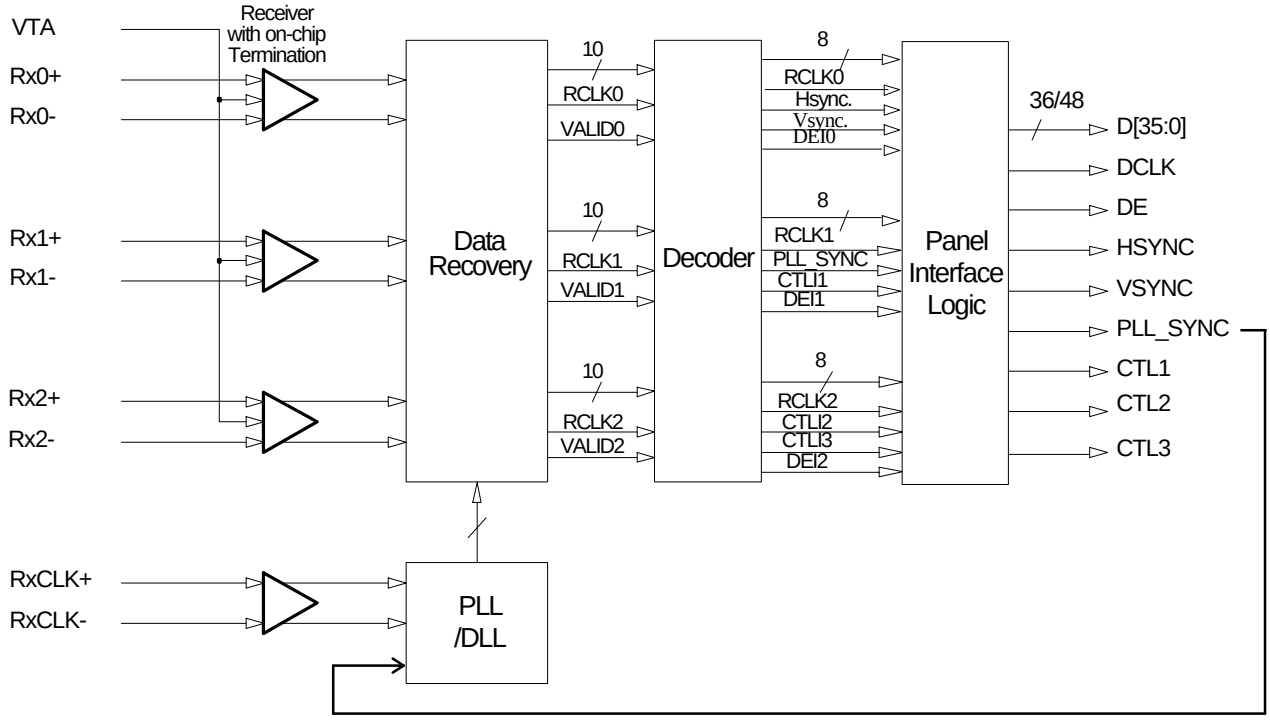


Figure 5.7: TMDS Receiver IC Functional Block Diagram

There can be inter-channel timing skew among the multiple channel data recovery blocks because the line length of different data transmission pairs can be slightly different. The inter-channel timing skew can produce up to 1 cycle time of mismatch.

The TMDS interface defines a logical architecture, an encoding scheme and a scaleable physical interface based on a low-voltage differential swing current-mode circuit technology. Up to 8 bits of colour data is carried on each differential data pair. Three (3) control signals can be used for implementation-dependent or user-defined signals.

5.1.6 Relationship Between Controller's Output Data and Input Data Clock

The vertical and horizontal timing diagrams in figures 5.8 → 5.12 for a typical Flat Panel Display Graphics Controller demonstrate the relationship between the controller's output data (D[23:0]) and the transmitter interface input data clock (IDCK).

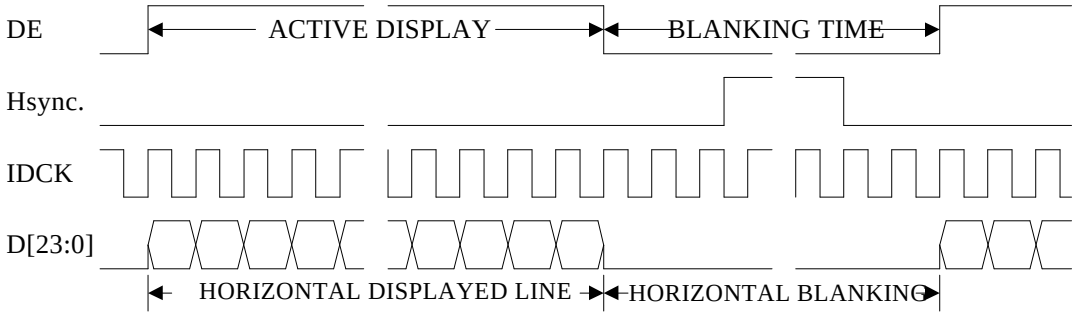


Figure 5-7 : Horizontal Input Timing at Type B Interface

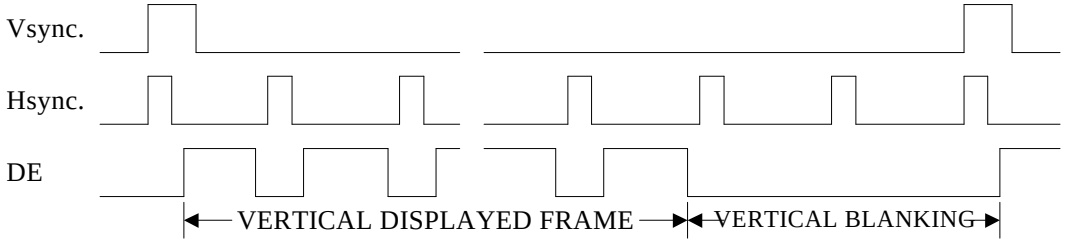


Figure 5-8 : Vertical Input Timing at Type B Interface

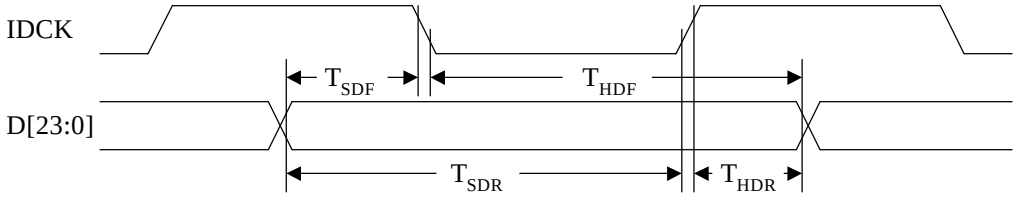


Figure 5-9 : Input Data Timing with Respect to IDCK at Type B Interface

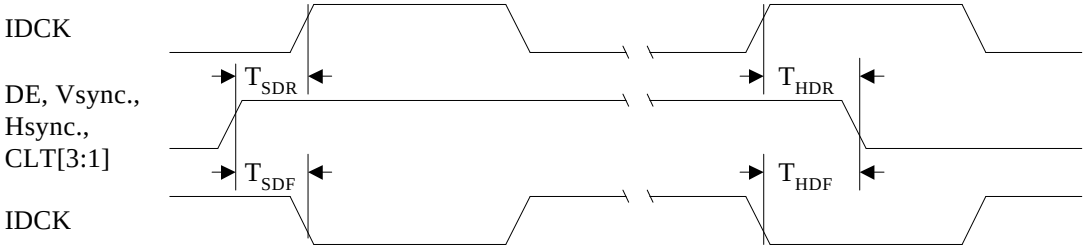


Figure 5-10 : Control Signal Timing with Respect to IDCK at Type B Interface

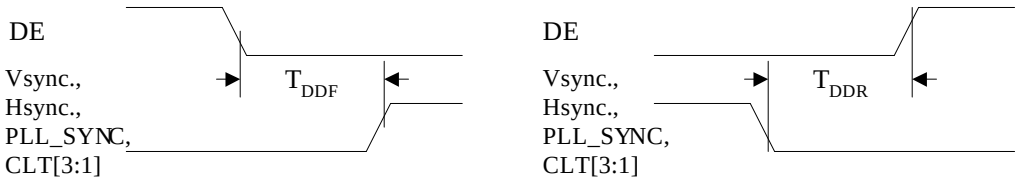


Figure 5-11 : Control Signals with Respect to DE Timing

Signal Name	Type	Description
Hsync.	In	Horizontal Sync. Input
Vsync.	In	Vertical Sync. Input
PLL_SYNC	In	General Input Control Signal 0 reserved for PLL_SYNC
CLT1	In	General Input Control Signal 1
CLT2	In	General Input Control Signal 2
CLT3	In	Stereo Sync. Input (optional)
DE	In	Input Data Enable. This signal qualifies the active data area. DE is always required and must be high for active video time and low during blanking.
IDCK	In	Input Data clock. Maximum frequency is 160 MHz. Input data can be valid either on falling edge of IDCK or on rising edge of IDCK as selected by DEDGE pin. IDCK must be a continuous free running clock with a minimum 40/60 or maximum 60/40 duty cycle.
DEDGE	In	Data Latching Edge for input data. A low level indicates that input data (D[23:0]) must be latched on falling edge of IDCK while a high level (3.3V) indicates that input data must be latched on rising edge of IDCK.
CEDGE	In	Control Latching Edge for input data enable (DE) and control signals (HSYNC, VSYNC, CLT[3-0]). A low level indicates that input data enable and control signals must be latched on falling edge of IDCK while high level (3.3V) indicates that input data enable and control signals must be latched on rising edge of IDCK.
Data	In	Input data is synchronised with input data clock (IDCK). Data can be latched on the rising or falling edge of IDCK depending upon whether DEDGE is high or low respectively.

Table 5-4 : Signal Name Descriptions

The clock line is not the same frequency as the data rate. The clock runs at $1/10^{th}$ of the maximum data rate.

In the above diagram DE, Hsync., and Vsync. signals are shown with positive polarity. DE must always have positive polarity, whereas Hsync., Vsync. and other control signals (CLT[3:1]) can have either positive or negative polarity. DE must always be connected and must go low for a minimum of 10 IDCK cycles, even for DSTN panels. The interface relies on the polarity and timing of DE and not on the control signals.

The Display Enable (DE) signal is used to differentiate between “active” display area and “non-active” display area (“blank” time). The interface requires an active high Display Enable (DE) signal. There is no restriction on the polarity of the control signals; however, the change in polarity for the control signals is only recognised during “blank” time.

Input data D[23:0] and Data Enable (DE) are normally generated on the rising edge of IDCK since most displays latch data on the falling edge of shift clock. For the interface, D[23:0] and DE can be latched on the rising or falling edge of IDCK depending upon the setting of DEDGE and CEDGE respectively. The DEDGE pin controls the latching of data D[23:0]. When DEDGE is low, D[23:0] is latched using the falling edge of IDCK. When DEDGE is high, D[23:0] is latched using the rising edge of IDCK. The CEDGE pin controls the latching of control signals DE, Hsync., Vsync., CLT[3:1]. When CEDGE is low, DE and the other control

signals are latched using the falling edge of IDCK. When CEDGE is high, DE and the other control signals are latched using the rising edge of IDCK.

The timing between D[23:0] and DE with respect to IDCK falling/rising edge, requires close attention. Timing considerations between the other control signals and IDCK are not as restrictive since the display timing requirements are relaxed.

For most Display Graphics Controllers, D[23:0] and DE have the same or similar timing; therefore, DEDGE and CEDGE should to be set at the same level. However, if D[23:0] is to be latched using the rising edge of IDCK and DE using the falling edge of IDCK, then DE will be latched half a clock cycle earlier with respect to D[23:0]. Subsequently, DE and D[23:0] are synchronised at the output of the data capture logic.

IDCK must always be free running with nominally 50/50 duty cycle and less than 5% jitter.

5.2 TMDS Transition-Controlled Digital Encoding and Signal Transmission

The encoder is required to encode 8-bits of data during active display time, and data enable (DE) + 2-bits of control signals during blank time. The encode is required to generate 10-bit DC-balanced and transition minimised codes during active display time. Control signals are assumed to change only during "blank" time when DE is low/inactive; the levels of the control signals are assumed to be constant during active data area when DE is high.

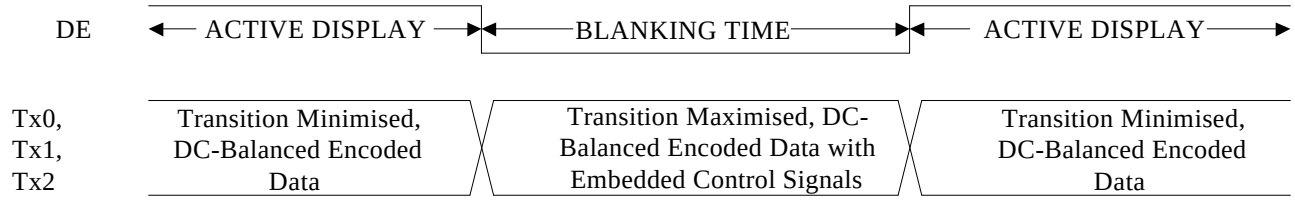


Figure 5-12 : TMDS Interface Transition Minimisation Timing Diagram

The encoding method guarantees transition-minimised DC-balanced 256 level data codes during active time during blank time, which supports high speed, low voltage differential, low power, and low EMI operation. The special characters are used for the level encoding of the control signals.

Encoded are 8-bits of data + data enable (DE) + 2-bits of control signals. The TMDS encoding method encodes the levels of control signals when DE is low. The encoding method guarantees the number of signal edge transitions in any 8-bits of date are minimised to no more than three (3) transitions and a DC balanced character set is generated for the data. Four kinds of special characters are used for the level encoding of the control signals. A total of 260 (256 in-band data set and 4 out-of-band special character set) 10-bit characters are conveyed for each encoded parallel data stream.

Data [7:0]	DE	VSYNC	HSYNC	10-bit code
1 to 256	High		-	C_1-C_{256}
-	Low	L	L	C_{257}
-	Low	L	H	C_{258}
-	Low	H	L	C_{259}
-	Low	H	H	C_{260}

Table 5-5 : Encoded Data Components for Tx0 Differential Data Pair

Data [7:0]	DE	PLL_SYNC	CLT1	10-bit code
1 to 256	High		-	C_1-C_{256}
-	Low	L	L	C_{257}
-	Low	L	H	C_{258}
-	Low	H	L	C_{259}
-	Low	H	H	C_{260}

Table 5-6 : Encoded Data Components for Tx1 Differential Data Pair

Data [7:0]	DE	CLT2	CLT3	10-bit code
1 to 256	High		-	C_1-C_{256}
-	Low	L	L	C_{257}
-	Low	L	H	C_{258}
-	Low	H	L	C_{259}
-	Low	H	H	C_{260}

Table 5-7 : Encoded Data Components for Tx2 Differential Data Pair

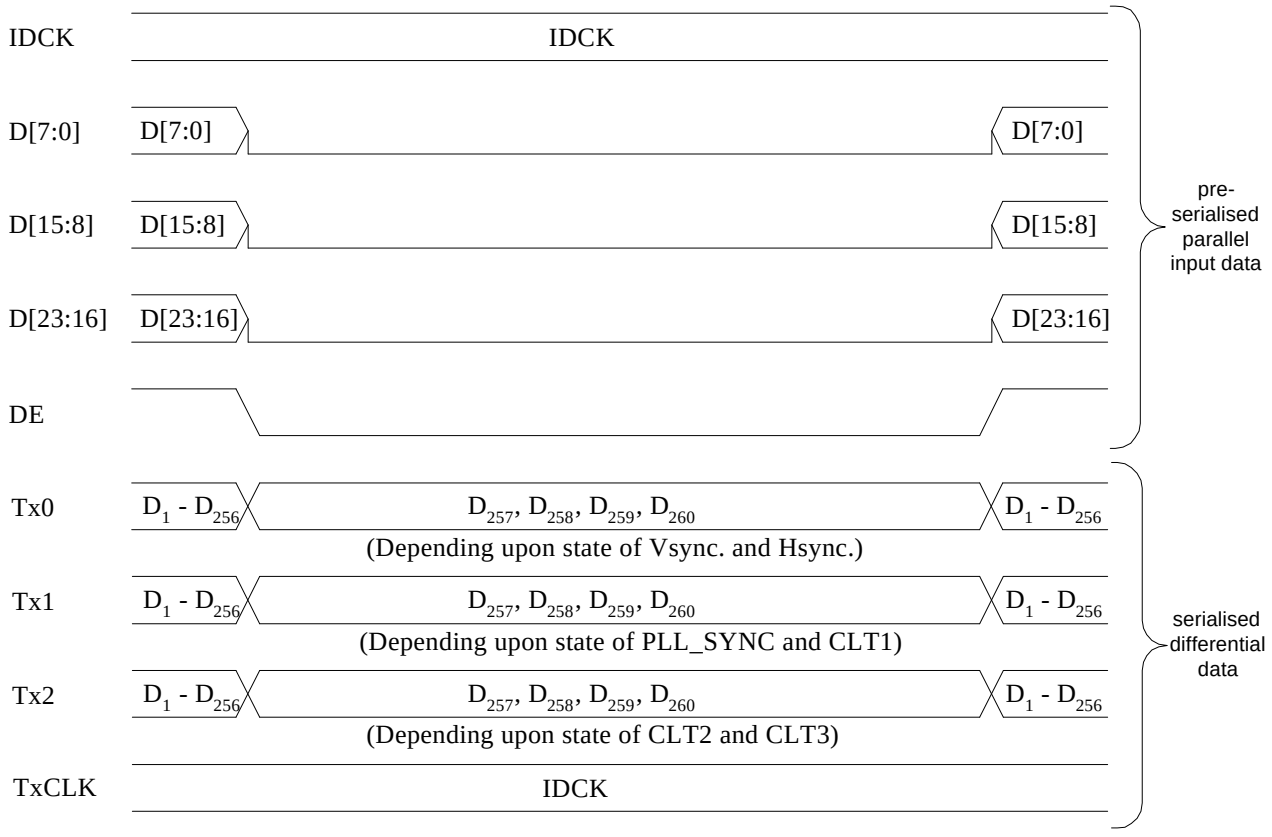


Figure 5-13 : Encoded Timing Diagram for All Differential Data Pairs

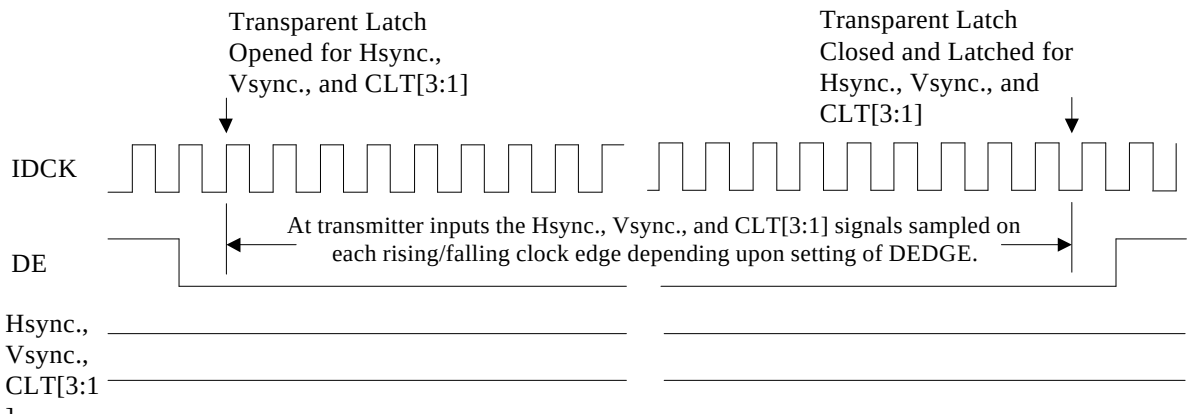


Figure 5-14 : Hsync., Vsync., and CTL[3:1] Sampling Relative to Clock Edge

A compliant implementation must generate one of the four kinds of special characters according to the level of Hsync. and Vsync. (or 2 control inputs) when DE is low. When DE is high, 8-bit data is converted to 10-bit transition minimised and DC-balanced in-band data. Four kinds of special characters are used for the level encoding of the control signal.

A compliant implementation is required to generate the 10-bit DC-balanced codes. Control signals are assumed to change only during “blank” time when DE is low/inactive; therefore, the levels of the control signals are allowed to be constant during active data area when DE is high.

A compliant implementation is required to generate one of four kinds of special characters depending upon the level of Hsync. and Vsync. or Control [3:1], when DE is low. When DE is high, 8-bit data is converted to 10-bit coded RGB data in each of 4 channels at the transmitter.

5.3 System Debug on Differential Data Pairs

The following will allow the system designer to generate a reproducible (triggerable) pattern for system debug on the differential data pairs. With Data Enable (DE) low the following out-of-band characters will be sent depending only on the sync. characters. This requires the sync. signals and DE be jumpered on the system designer's prototype board. The patterns are independent of the 24 bit data bus into the transmitter. The patterns will be decoded by the TMDS receiver.

Rx0 Differential Data Pair (e.g. blue):											
Hsync.	**Vsync.**	**d0**	**d1**	**d2**	**d3**	**d4**	**d5**	**d6**	**d7**	**d8**	**d9**
0	0	0	0	1	0	1	0	1	0	1	1
1	0	1	1	0	1	0	1	0	1	0	0
0	1	0	0	1	0	1	0	1	0	1	0
1	1	1	1	0	1	0	1	0	1	0	1
Rx1 Differential Data Pair (e.g. green):											
PLL_SYNC	**CTL1**	**d0**	**d1**	**d2**	**d3**	**d4**	**d5**	**d6**	**d7**	**d8**	**d9**
0	0	0	0	1	0	1	0	1	0	1	1
1	0	1	1	0	1	0	1	0	1	0	0
0	1	0	0	1	0	1	0	1	0	1	0
1	1	1	1	0	1	0	1	0	1	0	1
Rx2 Differential Data Pair (e.g. red):											
CTL2	**CTL3**	**d0**	**d1**	**d2**	**d3**	**d4**	**d5**	**d6**	**d7**	**d8**	**d9**
0	0	0	0	1	0	1	0	1	0	1	1
1	0	1	1	0	1	0	1	0	1	0	0
0	1	0	0	1	0	1	0	1	0	1	0
1	1	1	1	0	1	0	1	0	1	0	1

Table 5-8 : System Debug Patterns

Example: for DE = 0, Vsync. = 0, Hsync. = 0. Differential Data Pair Rx0 will cycle through the sequence 0010101011 repeatedly. The bit time will be the pixel clock period x10.

5.4 Implementation

Hsync. & Vsync. are transmitted via Tx0; PLL_SYNC & CLT1 are transmitted via Tx1; CLT2 & CLT3 are transmitted via Tx2. The Data is sent during active display time while the control signals are sent during blank time.

5.4.1 Amplitude Modulated Signal mapping (e.g. TFT)

Differential Data Pair #	18 bpp	Pixel Mapping	24 bpp	Pixel Mapping
Tx0	D[7:0]	D0 : unused	D[7:0]	D0 : B0
		D1 : unused		D1 : B1
		D2 : B0		D2 : B2
		D3 : B1		D3 : B3
		D4 : B2		D4 : B4
		D5 : B3		D5 : B5
		D6 : B4		D6 : B6
		D7 : B5		D7 : B7
Tx1	D[15:8]	D8 : unused	D[15:8]	D8 : G0
		D9 : unused		D9 : G1
		D10 : G0		D10 : G2
		D11 : G1		D11 : G3
		D12 : G2		D12 : G4
		D13 : G3		D13 : G5
		D14 : G4		D14 : G6
		D15 : G5		D15 : G7
Tx2	D[23:16]	D16 : unused	D[23:16]	D16 : R0
		D17 : unused		D17 : R1
		D18 : R0		D18 : R2
		D19 : R1		D19 : R3
		D20 : R2		D20 : R4
		D21 : R3		D21 : R5
		D22 : R4		D22 : R6
		D23 : R5		D23 : R7
TxCLK	DCLK		DCLK	

Table 5-9 : Amplitude Modulated Colour Mapping

5.4.2 Temporal Modulated Signal Mapping (e.g. DSTN) - 16bpp

Differential Data Pair #	16 bpp	Pixel Mapping 1st Transfer	Pixel Mapping 2nd Transfer	Pixel Mapping 3rd Transfer
Tx0	D[7:0]	D0 : UR0	D0 : UB2	D0 : UG5
		D1 : UG0	D1 : UR3	D1 : UB5
		D2 : UB0	D2 : UG3	D2 : UR6
		D3 : UR1	D3 : UB3	D3 : UG6
		D4 : LR0	D4 : LB2	D4 : LG5
		D5 : LG0	D5 : LR3	D5 : LB5
		D6 : LB0	D6 : LG3	D6 : LR6
		D7 : LR1	D7 : LB3	D7 : LG6
Tx1	D[15:8]	D8 : UG1	D8 : UR4	D8 : UB6
		D9 : UB1	D9 : UG4	D9 : UR7
		D10 : UR2	D10 : UB4	D10 : UG7
		D11 : UG2	D11 : UR5	D11 : UB7
		D12 : LG1	D12 : LR4	D12 : LB6
		D13 : LB1	D13 : LG4	D13 : LR7
		D14 : LR2	D14 : LB4	D14 : LG7
		D15 : LG2	D15 : LR5	D15 : LB7
Tx2	D[23:16]	D16 : SHFCLK	D16 : SHFCLK	D16 : SHFCLK
		D17 : n/c	D17 : n/c	D17 : n/c
		D18 : n/c	D18 : n/c	D18 : n/c
		D19 : n/c	D19 : n/c	D19 : n/c
		D20 : n/c	D20 : n/c	D20 : n/c
		D21 : n/c	D21 : n/c	D21 : n/c
		D22 : n/c	D22 : n/c	D22 : n/c
		D23 : n/c	D23 : n/c	D23 : n/c
TxCLK	DCLK			

Table 5-10 : Temporal Modulation Colour Mapping - 16bpp

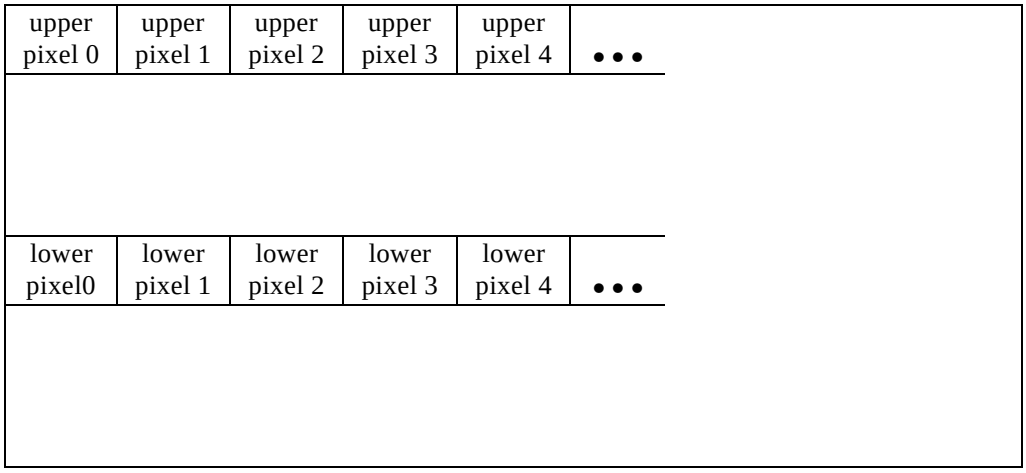


Table 5-11 : Temporal Mapping, Pixel Location on Display

5.4.3 Temporal-Modulated Signal Mapping (e.g. DSTN) - 24bpp

Differential Data Pair #	24 bpp	Pixel Mapping 1st Transfer	Pixel Mapping 2nd Transfer
Tx0	D[7:0]	D0 : UR0	D0 : UR4
		D1 : UG0	D1 : UG4
		D2 : UB0	D2 : UB4
		D3 : LR0	D3 : LR4
		D4 : LG0	D4 : LG4
		D5 : LB0	D5 : LB4
		D6 : UR1	D6 : UR5
		D7 : UG1	D7 : UG5
Tx1	D[15:8]	D8 : UB1	D8 : UB5
		D9 : LR1	D9 : LR5
		D10 : LG2	D10 : LG5
		D11 : LB2	D11 : LB5
		D12 : UR2	D12 : UR6
		D13 : UG2	D13 : UG6
		D14 : UB2	D14 : UB6
		D15 : LR2	D15 : LR6
Tx2	D[23:16]	D16 : LG2	D16 : LG6
		D17 : LB2	D17 : LB6
		D18 : UR3	D18 : UR7
		D19 : UG3	D19 : UG7
		D20 : UB3	D20 : UB7
		D21 : LR3	D21 : LR7
		D22 : LG3	D22 : LG7
		D23 : LB3	D23 : LB7
TxCLK	DCLK		

Table 5-12 : Temporal Modulation Colour Mapping - 24bpp

5.5 Physical Layer

5.5.1 Signal Bandwidth Characteristics

P_{CLK}	f_o MHz	x	f_c GHz	Maximum Distributed rise-time
25	125	3	0.375	933ps
40	200	3	0.600	583ps
65	325	3	0.975	360ps
112	560	3	1.68	208ps
160	800	3	2.4	145ps

Table 5-13 : Distributed Transmission Path Bandwidth and Rise-Time

Note:

P_{clk} = Pixel Clock

f_o = frequency operation

x = harmonic order

f_c = cut-off frequency = $3f_o$

rise time = $0.35/f_c$

6. Electrical Layer Specification: TMDS Transmission Specification

6.1 Electrical Characteristics

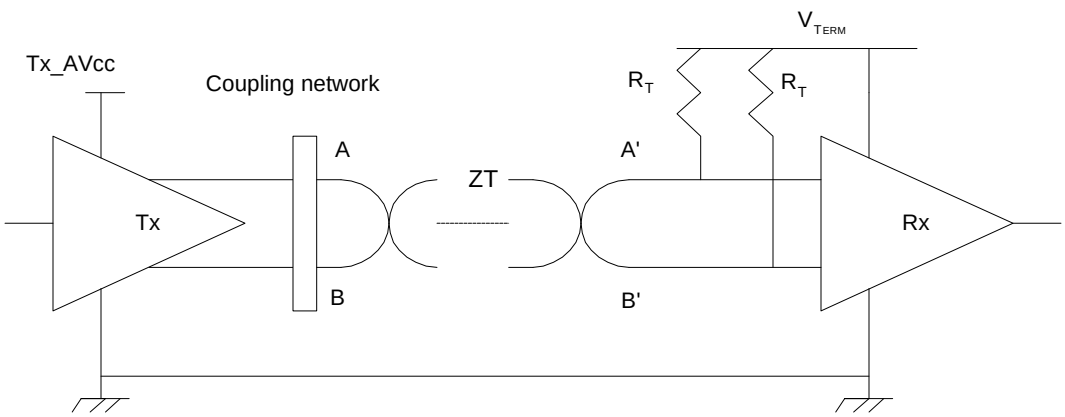


Figure 6-1 : Differential Mode Impedance

TxOUT = Transmitter — RxIN = Receiver
A = Transmitter interface point — A' = Receiver interface point
B = Transmitter interface point — B' = Receiver interface point
RT = Termination Resistance — V_{TERM}= Termination Voltage
Tx_AVcc = 3.3V ± 5% (with capacitor coupling)
V_{TERM} = 3.3V ± 5% (with capacitor coupling)
$90\Omega < Z_T < 110\Omega$ (range of allowed differential mode impedance of the media.)
$Z_T = 100\Omega$ for P&D
$R_T = ½ Z_T$
I_{SINK} = 12mA for A/A' or B/B'
$100mV < V_{SWING} < 600mV$ single-ended with $R_T = 50\ \Omega$ on A or B.

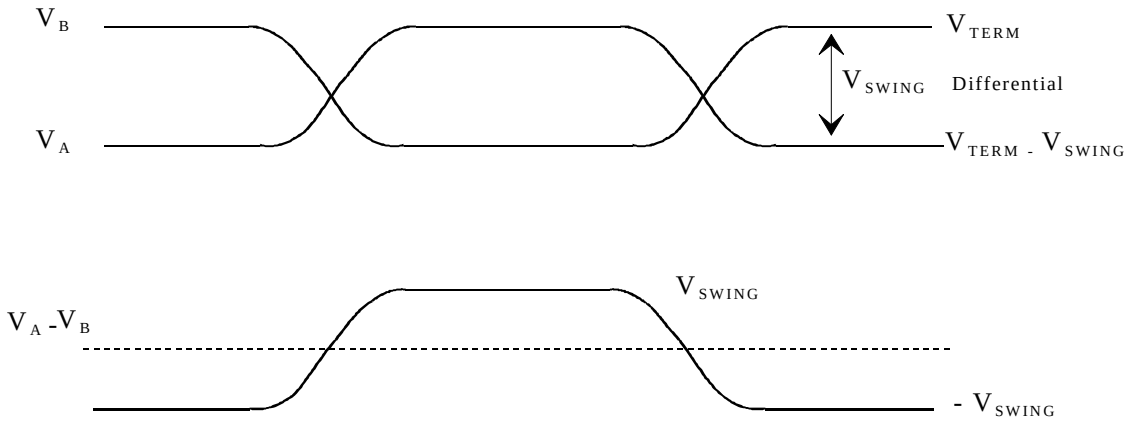


Figure 6-2 : Signal Levels on Transmission Media

6.2 DC Electrical Specifications

DC specifications for both driver and receiver are given in Table 6.1.

6.2.1 Differential Transmitter DC Specifications

(Under Normal Operating Conditions).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Output Voltage	R_L = 50Ω, R_{TX} = 500Ω	483	521	567	mV
		R_L = 50Ω, R_{TX} = 850Ω	269	295	331	mV
V_{OH}	High-level Output Voltage	Z_0 = 50Ω	3.2	3.25	3.3	V
V_{OL}	Low-level Output Voltage	R_L = 50Ω, R_{TX} = 500Ω		2.73		V
		R_L = 50Ω, R_{TX} = 850Ω		2.96		V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V			5	mA
I_{OZ}	Output Tri-state Current	PD# = 0, V_{OUT} = V_{CC}		+/- 4	+/- 11	µA
I_{CCT}	Transmitter Supply Current	DCLK = 65 MHz			62	mA
	@ 3.3V V_{CC}	DCLK = 40 MHz			38	mA
I_{PD}	Power-down Current				100	µA

Table 6-1 : Transmitter DC Specifications for 25 - 65MHz

6.2.2 Differential Receiver DC Specifications

(Under Normal Operating Conditions).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High-level Output Voltage	OVCC = 3.3V		3.3		V
		OVCC = 5V		5		
V_{OL}	Low-level Output Voltage		GND	0.1	0.25	V
I_{OHD}	Output High Drive	V_{OUT} = V_{OH} , Data and Controls		12.4		mA
I_{OLD}	Output Low Drive	V_{OUT} = V_{OL} , Data and Controls		18.32		mA
I_{OHC}	Output High Drive	V_{OUT} = V_{OH} , ODCK		27.3		mA
I_{OLC}	Output Low Drive	V_{OUT} = V_{OL} , ODCK		40.1		mA
V_{ID}	Differential Input Voltage		250	600	1000	mV
I_{CCR}	Receiver Supply Current	DCLK = 65 MHz			90	mA
	@ 3.3V V_{CC}	DCLK = 40 MHz			55	mA
I_{PD}	Power-down Current				100	µA

Table 6-2 : Receiver DC Specifications for 25 - 65MHz

Symbol	Parameter	Conditions	Min	Max	Unit
I_{OH}	Output current high	V_{TERM} = 3.3 V	2	12	mA
		R_{TERM} = 50 Ω			
I_{OL}	Output current low	V_{TERM} = 3.3 V		0.1	mA
		R_{TERM} = 50 Ω			
V_{TERM}	Termination voltage	R_{TERM} = 50 Ω	2.4	4.2	V
R_{TERM}	Termination resistance	V_{TERM} = 3.3 V	45	55	Ω
V_{ID}	Input differential voltage		100		mV

Table 6-3 : DC Specifications

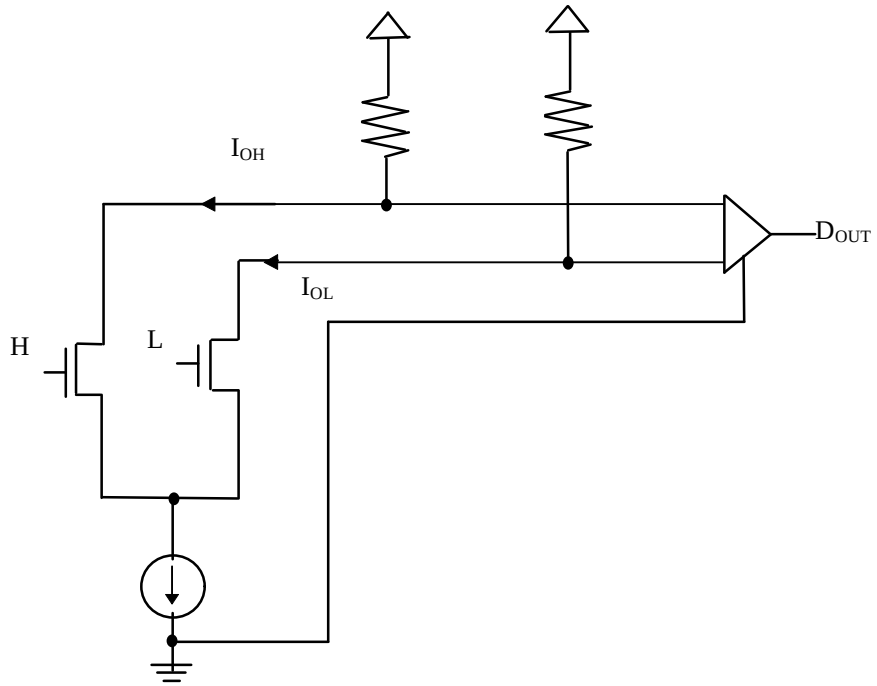


Figure 6-3 : Test Circuit for Measuring I_{OH} and I_{OL}

Note: I_{OH} and I_{OL} should be measured as close to the TMDS transmitter pins as practical.

6.3 Driver Output Levels

Driver output stage is a differential current switch with externally adjustable current. The range of adjustment is from 2mA to 12mA, depending on the length of the cable. The output impedance of the driver is dominant compared with the characteristic impedance of the interconnect media. Thus, the output current is not affected by the termination voltage. Impedance of the interconnect is 100Ω with 10% tolerance. 50Ω termination resistors with 10% tolerance are connected to the receiver supply voltage.

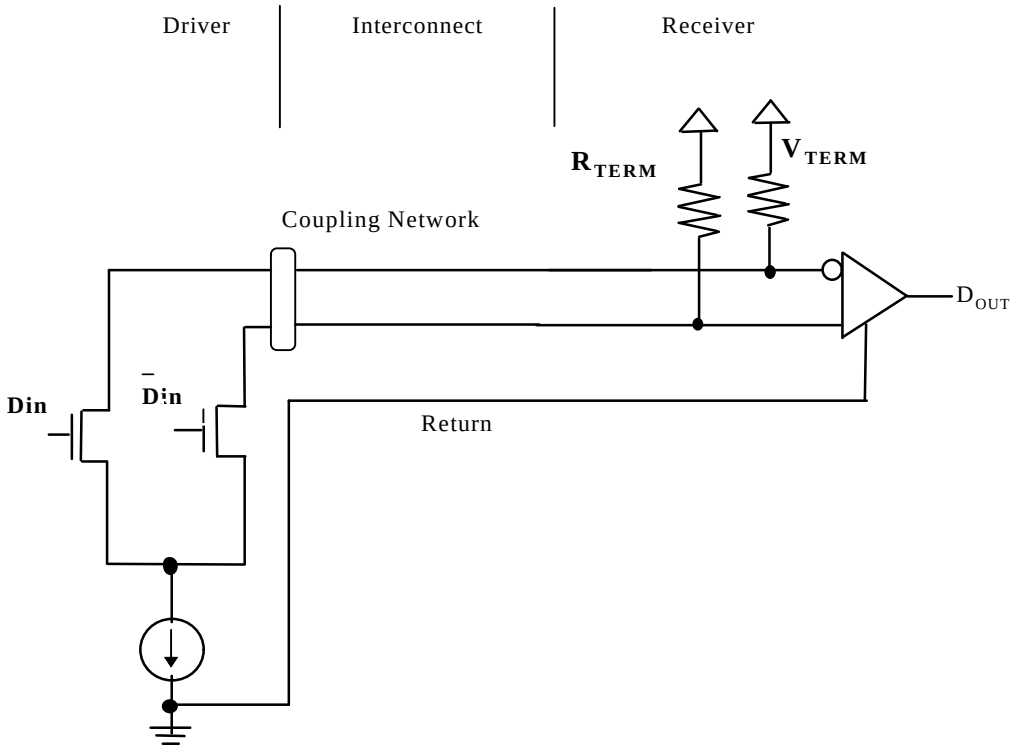


Figure 6-4 : Driver and receiver Circuit Model for One Differential Data Pair

Test Circuit Information: Din = High ; $\overline{\text{Din}}$ = Low

I_{OH} = 12mA for P&D

Figure 6.5 shows the DC signal levels of the driver and receiver in the presence of voltage shift between ground levels of the driver and receiver. A maximum of 0.6V shift is allowed when AVcc is shared, which will cover most of the typical interconnect environment. However, when the cable is very long or fiber optic transmission is used, a.c. coupling is required. A typical circuit is shown in figures 6.6. Signal current must be increased in case of signal loss due to cable resistance to give the same signal level in the receiver. The receiver needs to be able to resolve 100mV differential input.

The P&D standard requires use of capacitor coupling between the TMDS transmitter and receiver, see figure 6.5

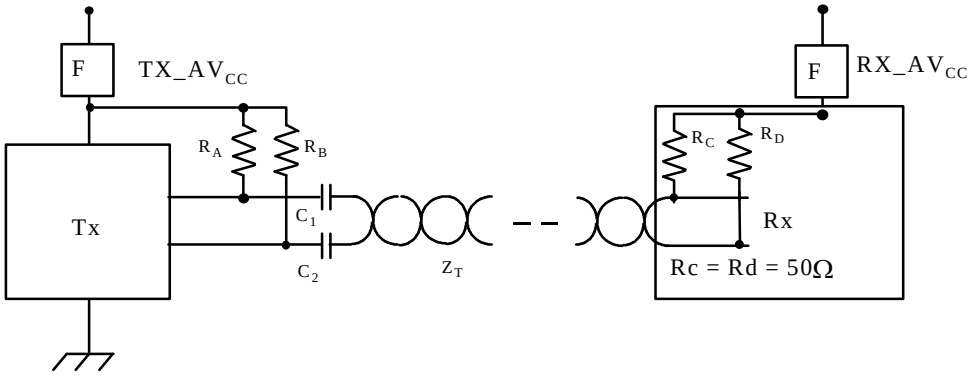


Figure 6-5 : Capacitor Coupled TMDS System

The purpose of R_A and R_B is to provide an average DC level on the TX side and provide source termination. R_C & R_D are on-chip termination resistors in the TMDS receiver.

Note: $R_A = R_B = ½ Z_T$, with $Z_T = 100Ω$, $T_{CLK} = 25MHz - 112MHz$, $C_1 = C_2$, $1nF < C_1 < 100nF$
$R_C*RX\_AV_{CC} = R_D*RX\_AV_{CC}=1/2V_{SWING}$

	25 - 65 MHz	**65 - 112 MHz**
Z_T	100 Ω	100 Ω
C_1	10 nF +/- 20% [1]	10 nF +/- 20% [1]
C_2	10 nF +/- 20% [1]	10 nF +/- 20% [1]
R_A	100 Ω	100 Ω
R_B	100 Ω	100 Ω
R_C	50 Ω	50 Ω
R_D	50 Ω	50 Ω

Table 6-4 : Component Values, Capacitor Coupling

[1] Typical p/n CE103X2NV

6.4 Signal Integrity

Maximum transmission rate is defined by the user depending on the application. In case of 800x600, a 40MHz dot clock is used. In case of 1024x768 and 1280x1024, 65MHz and 112 MHz could be used. A bit time is one tenth of a clock period. The duty cycle of the transmitted clock should be maintained close to 50% to remove DC component.

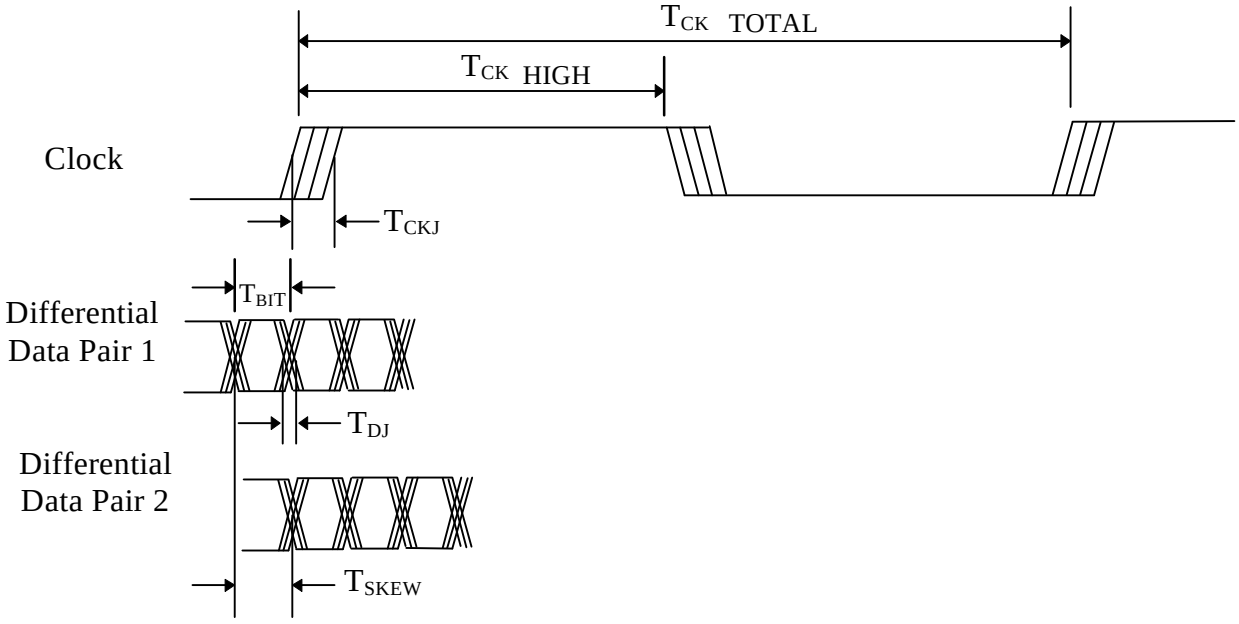


Figure 6-6 : Timing Diagram for Jitter and Skew Specification

6.4.1 Jitter and Skew of Clock and Differential Data Pairs

The amount of jitter in the dot clock is allowed within 5% of the dot clock period. For differential data pairs, 20% jitter with respect to bit time is allowed. The skew among the differential data pair is allowed within one bit time. Skew between clock and data channels is allowed within one bit time.

Frequency of Pixel Clock		**25MHz**	**40MHz**	**65MHz**	**112MHz**	**160MHz**
T_{CK}	= Clock Period = 1/F	40 ns	25 ns	15.38 ns	8.929 ns	6.25 ns
T_{CKH}	= Clock duty min/max	40/60	40/60	40/60	40/60	40/60
T_{CKJ}	= Clock jitter = T_{CK} x 0.05	2 ns	1.25 ns	769 ps	446 ps	313 ps
T_{BIT}	= Bit time = T_{CK} x 0.10	4 ns	2.5 ns	1.538 ns	892 ps	625 ps
T_{DJ}	= Data jitter = T_{BIT} x 0.20	800 ps	500 ps	307.6 ps	178.4 ps	125 ps
T_{SKEW}	= T_{BIT}	4 ns	2.5 ns	1.538 ns	892 ps	625 ps

Table 6-5 : Signal Integrity Parameters

6.5 Eye Diagram Template

The reference points for all connections between transmitter and receiver are points S and R as shown in Figure 6.7.

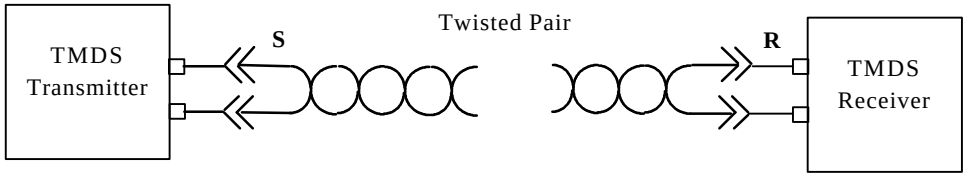


Figure 6-7: TMDS Connection

The output from the TMDS transmitter shall have the output levels as specified in section 7.7. The mask of the transmitter eye diagram as measured at the input to the cable (point S) on two 50Ω termination resistors, are given in Figure 6.8 and Table 6.6. The Y1 and Y2 amplitudes in Table 6.6 are set to allow overshoot and undershoots relative to the amplitudes of a logic 1 and 0.

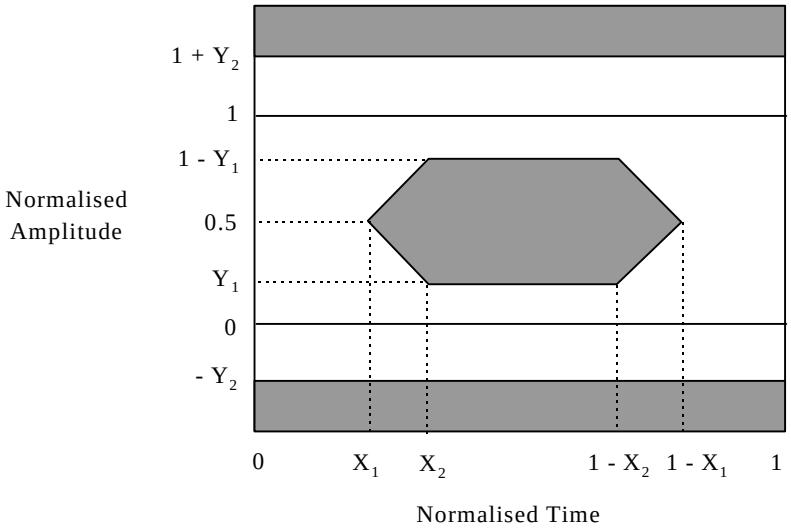


Figure 6-8: Eye Diagram Mask at Point S

DOT CLOCK FREQUENCY	X_1	X_2	Y_1	Y_2
25 MHz	0.15	0.25	0.20	0.20
40 MHz	0.15	0.25	0.20	0.20
65 MHz	0.20	0.30	0.20	0.20
112 MHz	0.20	0.30	0.20	0.20

Table 6-6 : Eye Diagram Mask at Point S[1]

[1] Preliminary

The TMDS receiver terminates the link by an equivalent resistance of 100Ω. The mask of the receiver eye diagram is given in Figure 6.9 and it's specification in Table 6.7.

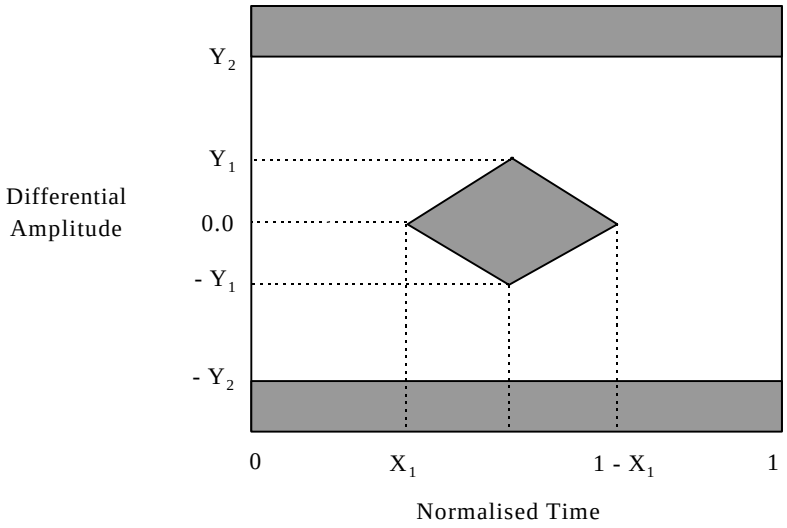


Figure 6-9: Eye Diagram Mask at Point R

DOT CLOCK FREQUENCY	X_1	Y_1	Y_2
25 MHz	0.30	100mV	600mV
40 MHz	0.30	100mV	600mV
65 MHz	0.30	100mV	600mV
112 MHz	0.30	100mV	600mV

Table 6-7: Eye Diagram Mask at Point R[1]

[1] Preliminary

6.6 AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
S_{LHT}	Small Swing Low-to-High Transition Time	C_L = 5pF	0.25	0.3	0.5	ns
S_{HLT}	Small Swing High-to-Low Transition Time	C_L = 5pF	0.25	0.3	0.5	ns
D_{LHT}	Digital Output Low-to-High	C_L = 15pF				
	Transition Time (Data, DE,	OVCC = 3.3V	2.5	3.1	4.1	ns
	Vsync., Hsync., CLT[3:0])	OVCC = 5.0V	1.9	2.4	3.0	ns
	(ODCK)	C_L = 15pF				
		OVCC = 3.3V	1.2	1.4	1.9	ns
		OVCC = 5.0V	0.9	1.1	1.4	ns
D_{HLT}	Digital Output High-to-Low	C_L = 15pF				
	Transition Time (Data, DE,	OVCC = 3.3V, Data Out	1.1	1.9	2.6	ns
	Vsync., Hsync., CLT[3:0])	OVCC = 5.0V, Data Out	1.3	1.6	2.1	ns
	(ODCK)	C_L = 15pF				
		OVCC = 3.3V, Clock Out	0.7	0.9	1.2	ns
		OVCC = 5.0V, Clock Out	0.6	0.7	0.9	ns
T_{LPL}	PLL Locking Time				12	us
T_{UPL}	PLL Unlocking Time				1	us
T_{DPS}	Differential Pair Skew	1 Bit Time			5	%
T_{CCS}	Differential data pair-to-Differential data pair Skew				T_{CIP}	ns
T_{CIP}	IDCK Cycle Time		15		40	ns
T_{CIH}	IDCK High Time		$0.4T_{CIP}$	$0.5T_{CIP}$	$0.6T_{CIP}$	ns
T_{CIL}	IDCK Low Time		$0.4T_{CIP}$	$0.5T_{CIP}$	$0.6T_{CIP}$	ns
T_{IJIT}	IDCK Jitter	$(0.05)x\ T_{CKJ}$			1	ns
R_{CIP}	ODCK Cycle Time		15		40	ns
R_{CIH}	ODCK High Time		$0.4T_{CIP}$	$0.5T_{CIP}$	$0.6T_{CIP}$	ns
R_{CIL}	ODCK Low Time		$0.4T_{CIP}$	$0.5T_{CIP}$	$0.6T_{CIP}$	ns

Table 6-8 : AC Specification (part 1)

Note: All timing measured from 80% and 20% of waveform signal.

Symbol	Parameter	Conditions	Min	Max	Unit
T_{SDF}	Data, DE, Vsync., Hsync., and CLT[3:0] Setup Time from IDCK falling edge	CEDGE = 0 DEDGE = 0	3		ns
T_{HDF}	Data, DE, Vsync., Hsync., and CLT[3:0] Hold Time from IDCK falling edge	CEDGE = 0 DEDGE = 0	4		ns
T_{SDR}	Data, DE, Vsync., Hsync., and CLT[3:0] Setup Time from IDCK rising edge	CEDGE = 1 DEDGE = 1	4		ns
T_{HDR}	Data, DE, Vsync., Hsync., and CLT[3:0] Hold Time from IDCK rising edge	CEDGE = 1 DEDGE = 1	3		ns
T_{DDF}	Vsync., Hsync., and CLT[3:0] Delay from DE falling edge		T_{CIP}		ns
T_{DDR}	Vsync., Hsync., and CLT[3:0] Delay from DE rising edge		T_{CIP}		ns
T_{TRX}	Differential Clock Output delay from IDCK			5.8	ns
T_{HDE}	DE high time			$8000T_{CIP}$	ns
T_{LDE}	DE low time		$10T_{CIP}$		ns
T_{PH1}	PLL_SYNC Delay from Vsync. asserted (Phase 1)	SYNC_CONT = 1	T_{CIP}	$3T_{CIP}$	ns
T_{PH2}	PLL_SYNC Delay from Vsync. asserted (Phase 2)	SYNC_CONT = 0	T_{CIP}	$3T_{CIP}$	ns
T_{LPS}	PLL_SYNC Delay from Vsync. de-asserted		T_{CIP}	$2T_{CIP}$	ns
T_{LPD}	Delay from PD Active to Outputs Disabled		4	6	ns
T_{HPD}	Delay from PD Inactive to Outputs enabled		4	6	ns

Table 6-9 : AC Specification (part 2)

Note : All timing measured from 80% and 20% of waveform signal.

6.6.1 Timing Diagrams

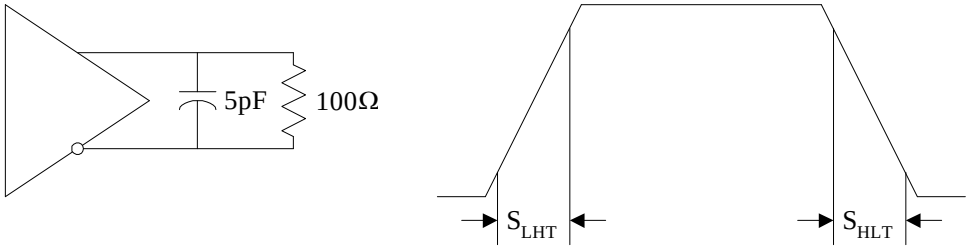


Figure 6-10 : Transmitter Small Signal Transition Times

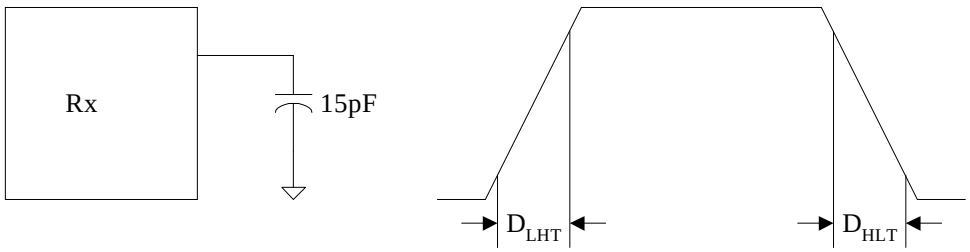


Figure 6-11 : Receiver Digital Output Transition Times

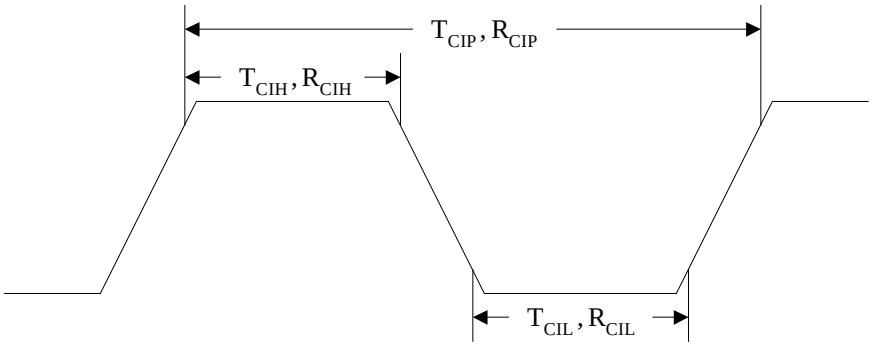


Figure 6-12 : Transmitter / Receiver Clock Cycle High / Low Times

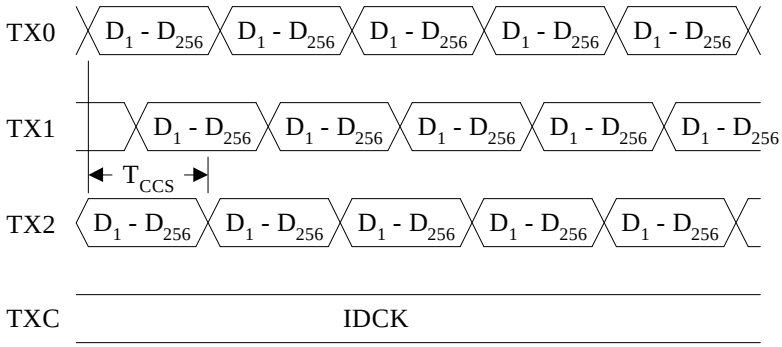


Figure 6-13 : Differential Data Pair to Differential Data Pair Skew Timing

6.6.1.1 Parallel Stream Input Timing to Transmitter

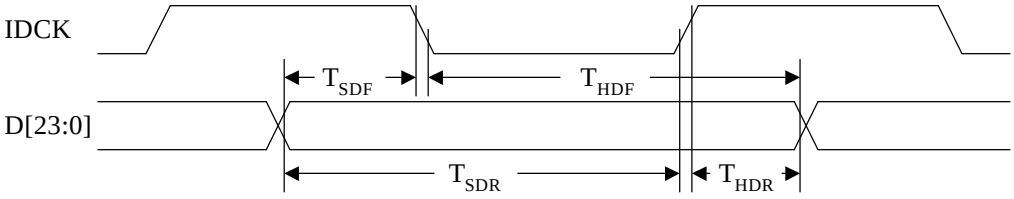


Figure 6-14 : DE, Vsync., Hsync., and CLT[3:1] Setup / Hold Times to IDCK of Transmitter

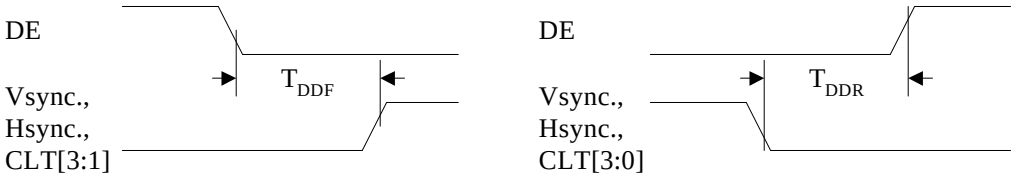


Figure 6-15 : Vsync., Hsync., and CLT[3:1] Delay Times from DE of Transmitter

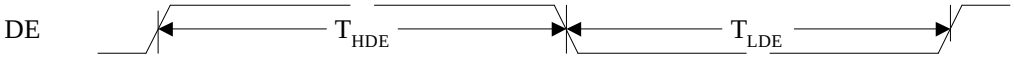


Figure 6-16 : DE High / Low Times of Transmitter

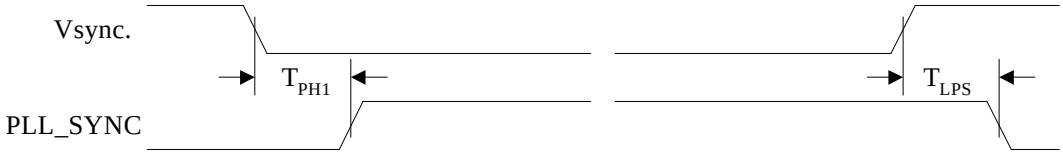


Figure 6-17 : PLL_SYNC Timing of Transmitter with SYNC_CONT = 1

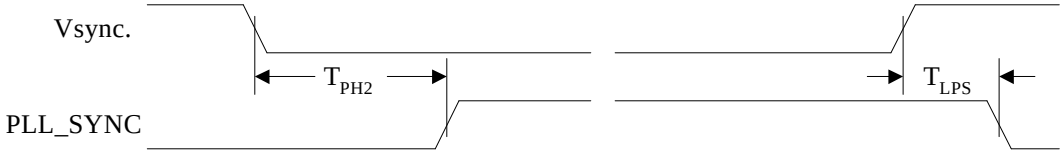


Figure 6-18 : PLL_SYNC Timing of Transmitter with SYNC_CONT = 0

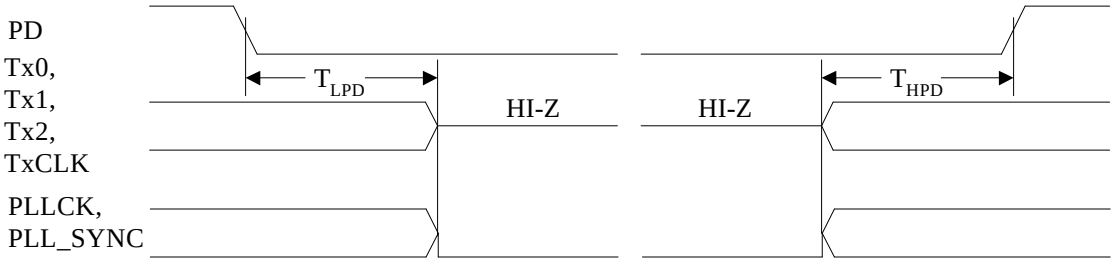


Figure 6-19 : Output Signals Disabled / Enabled Timing from PD Active / Inactive from Transmitter

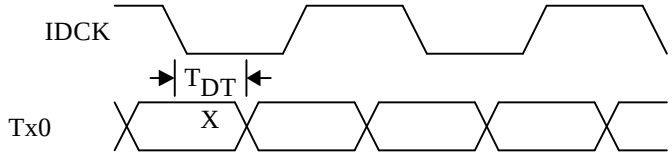


Figure 6-20 : Differential Clock Delay from IDCK

6.7 Error Specification for Display Interface

Pixel Error Rate[1] 1 pixel error / 2,000 frames (33 seconds at 60fps)

Hsync. and Vsync. pulses are spread over a number of frames determined by the length of the pulse. The pixel error rate is over one frame hence it is unlikely that a transmission error will affect more than a small percentage of the Hsync. or Vsync. pulse time.

6.8 Guidance for Display Controller Implementation

Line Error Rate[2] 1 pixel wide bit error / 20,000 frames (5 min 33 seconds at 60fps))
Full Frame Error Rate[3] 1 pixel wide bit error / 200,000 frames (55 min 33 seconds at 60 fps)

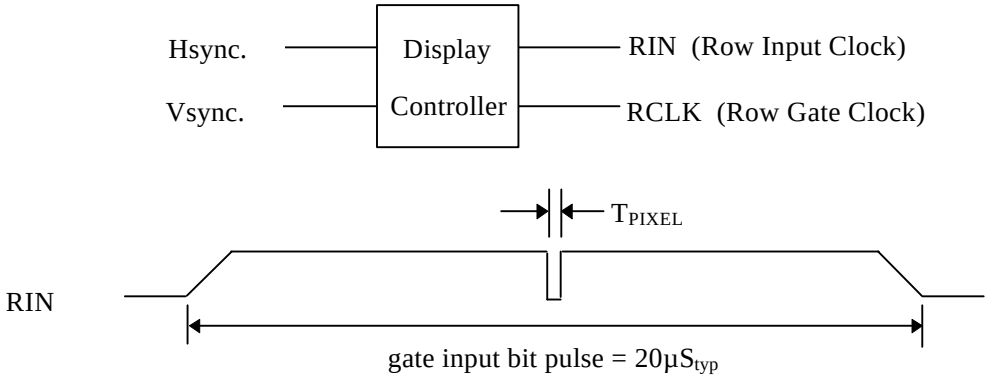


Figure 6-21 : Line Error Rate

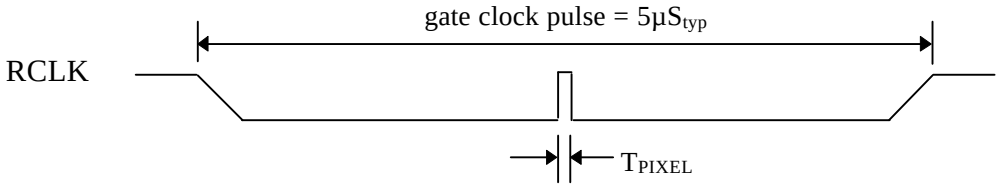


Figure 6-22 : Full Frame Error Rate

Possible display effects without fault tolerant logic:

- Pixel error rate results in single pixel error.
- Line error rate results in display of erroneous data on one line.
- Full frame error rate results in one frame with random data displayed.

7. Mechanical Physical Layer: Connector

7.1 Introduction

The P&D connector mating interface is covered by patents issued to Molex Inc. To obtain license to these patents and to obtain additional connector interface design detail companies should contact Molex Inc. directly.

This section describes the standardised P&D-A/D receptacle connector interface required on the host system (personal computer, workstation, etc.). For reference, information is also provided for the mating plug connector and for the P&D-D (digital only) receptacle and plug. The cable attached plug connectors provide the interconnection from the display device to the host.

General dimensions and tolerances, and description of those features which affect the intermateability of the receptacle and plug connectors are described in this section. The panel cutout, printed circuit board hole pattern, pinouts, performance characteristics and test criteria for the receptacle connector are also described in this section.

All other features which do not affect the intermateability are not described, and may vary. Definition of the cable assembly and cable can be found in Sections 8 and 9 respectively. Additionally, recommended cable assemblies for a digital interface monitor are provided in Appendix A (Section 10).

7.1.1 P&D-A/D Connector

The P&D-A/D connector contacts are separated into two primary groups. One set of 30 contacts, on 1.905 x 1.905 mm spacing, is designed to handle power, ground, digital, and low frequency analogue signals. The other set of 4 quasi-coaxial contacts is designed for high frequency, 75Ω, analogue signals.

Refer to figure 7.1 for the mating features and figure 7.3 for the pinouts.

7.1.2 P&D-D Connector

The P&D-D connector contacts are in a single group of 30 contacts, on 1.905 x 1.905 mm spacing, is designed to handle power, ground, digital, and low frequency analogue signals.

Refer to figure 7.2 for the mating features and figure 7.4 for the pinouts.

7.2 Receptacle Connector

Figure 7.1 provides basic dimensional information for the mating interface of the P&D-A/D receptacle connector and figure 7.2 provides basic dimensional information for the mating interface of the P&D-D receptacle connector. This information in addition to the mating information provided with the license will assure intermateability of the plugs with standardised receptacles. The receptacle is defined as the connector with the fully shrouded redundant contact point female contacts.

For reference, the recommended panel cutout for mounting both receptacles is included as figure 7.5.

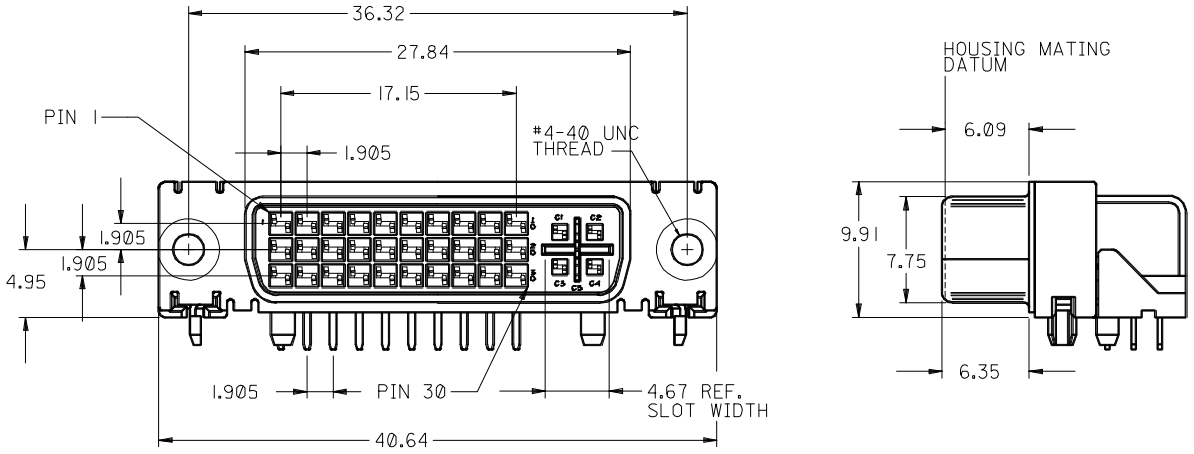


Figure 7-1 : P&D-A/D Receptacle Connector - Basic Mating Interface Dimensions

Notes:
1. Dimensions are in mm.
2. Interpret dimensions and tolerances per ASME Y14.5M - 1994.
3. Illustrations are in third angle projection.
4. Not to scale.

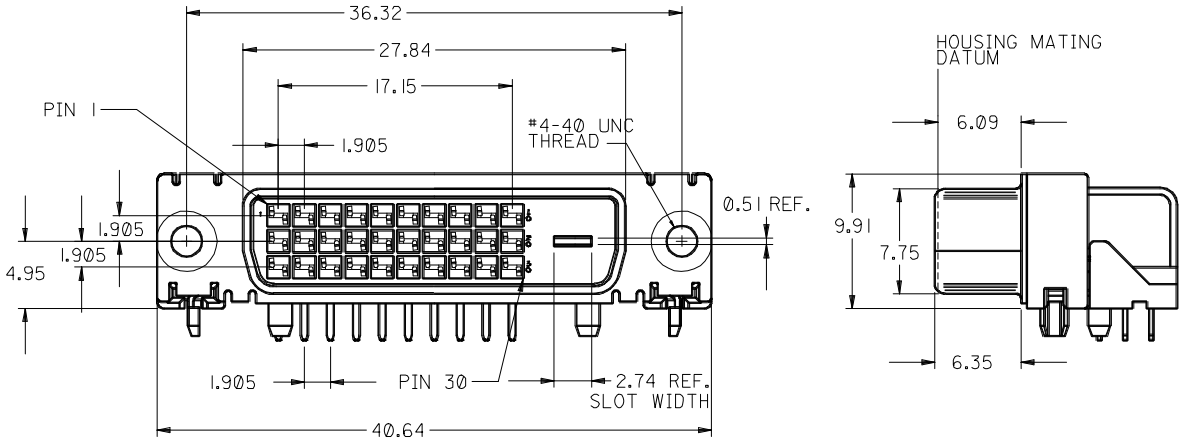


Figure 7-2 : P&D-D Receptacle Connector - Basic Mating Interface Dimensions

Notes:
1. Dimensions are in mm.
2. Interpret dimensions and tolerances per ASME Y14.5M - 1994.
3. Illustrations are in third angle projection.
4. Not to scale.

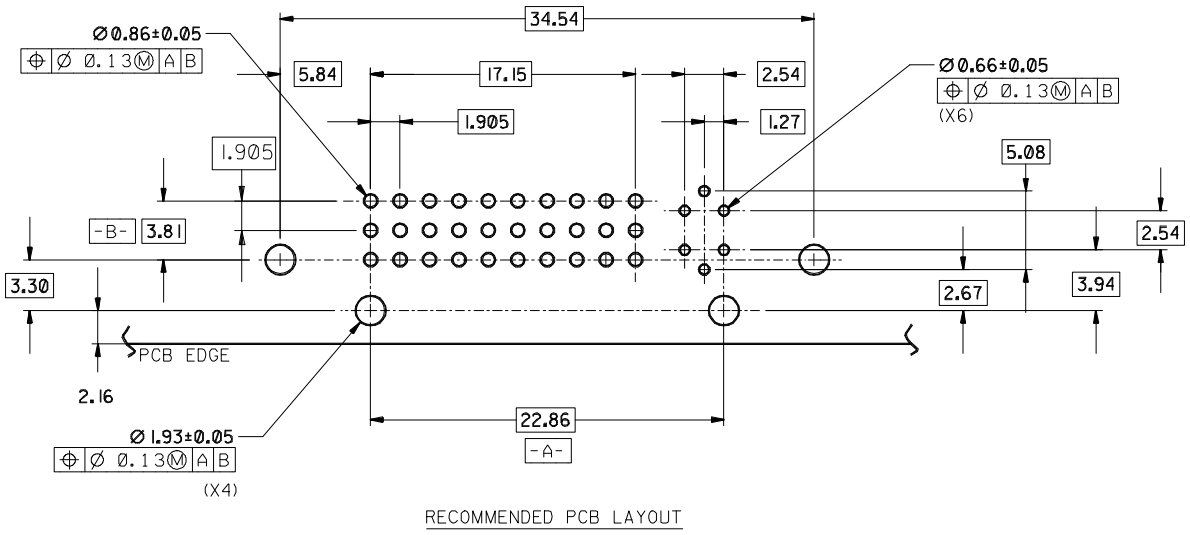


Figure 7-3 : P&D-A/D reference Hole Pattern (Receptacle)

Notes:
1. Dimensions are in mm.
2. Interpret dimensions and tolerances per ASME Y14.5M - 1994.
3. Not to scale.

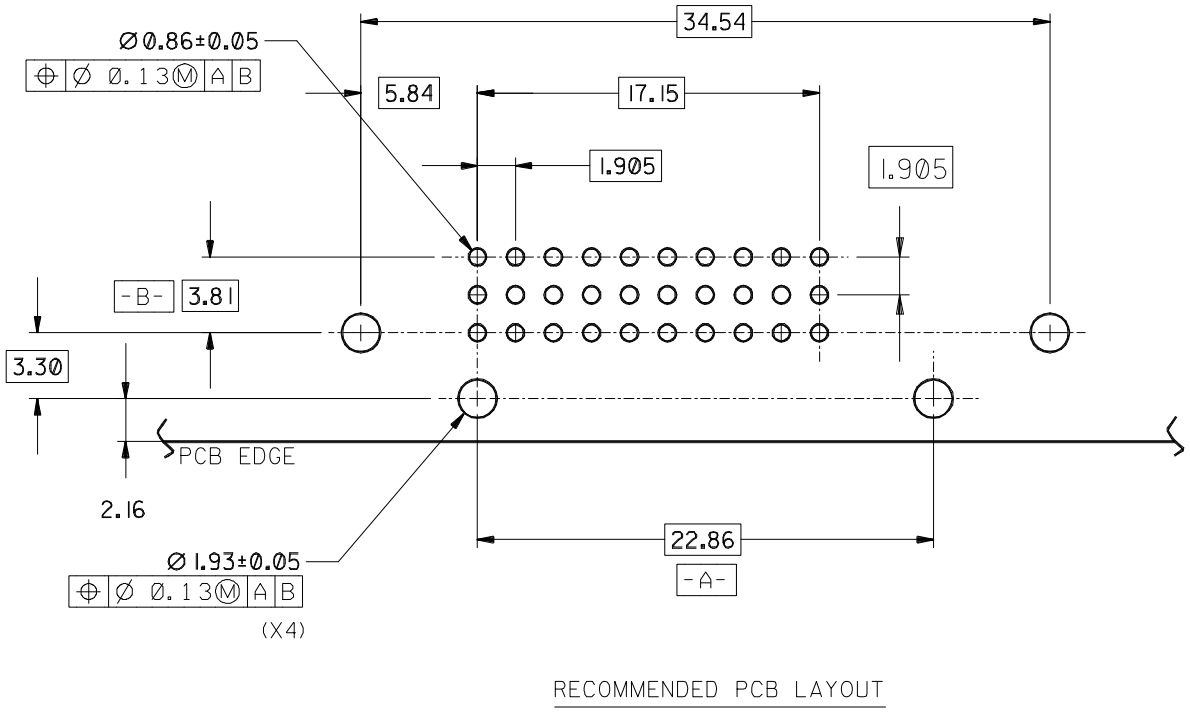


Figure 7-4 : P&D-D Reference Hole Pattern (Receptacle)

Notes:
1. Dimensions are in mm.
2. Interpret dimensions and tolerances per ASME Y14.5M - 1994.
3. Not to scale.

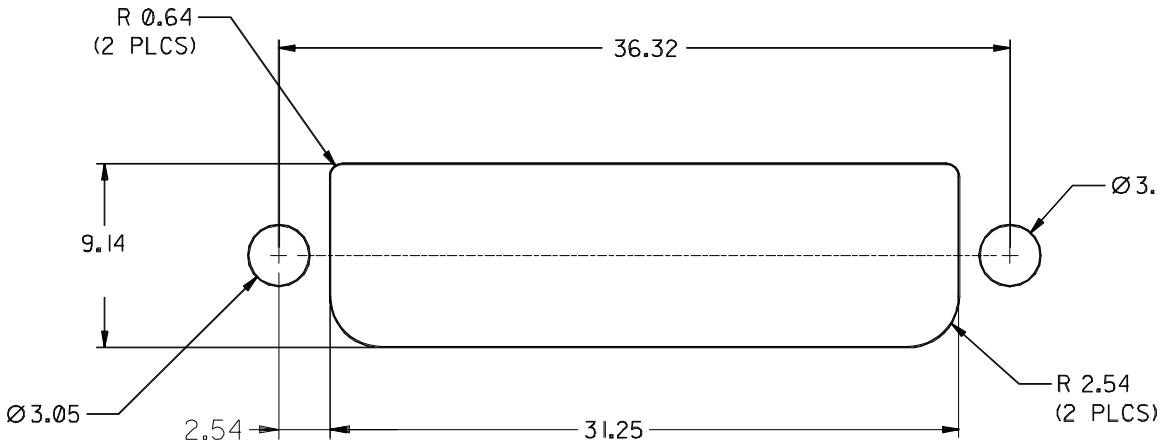


Figure 7-5 : Recommended Panel Cut-out

Notes:
1. Dimensions are in mm.
2. Interpret dimensions and tolerances per ASME Y14.5M - 1994.
3. Not to scale.

7.3 Positive Retention of Plug and Receptacle

Jackscrews with 4-40 threads are used to retain the plug and receptacle together and also to ensure that the plug and receptacle reference surfaces always bottom against each other during mating, thus providing an effective seal for EMC/RFI purposes.

7.4 Contact Finish On Plug And Receptacle Contacts

It is necessary to standardise the electroplated finish on the contacts to assure the performance and compatibility of the mating interfaces of the plugs and receptacles from different sources. The following standardised electroplatings are most common, but other thicknesses and compositions may be used providing they meet the test criteria in Section 7.10.

a) 0.76µm minimum gold, over 1.27µm nickel.
b) 0.25µm minimum gold over 0.76µm palladium-nickel alloy [1]80% Pd-20% Ni, over 1.27µm nickel

[1]Note: It is not acceptable to use tin, tin/lead, nickel or other non-noble materials known to be incompatible with gold or other essentially noble interfaces.

7.5 Shell Finish On Plugs And Receptacles

It is necessary to standardise the plated finish on the shells to insure compatibility of products from different sources. Both shells shall be electroplated with a minimum of 3.03µm of tin or tin alloy over a suitable underplate.

7.6 Connector Durability

The requirements of different end-use applications call for connectors which can be mated and unmated a different number of times, without degrading performance beyond acceptable limits. Accordingly, this standard establishes a minimum performance criteria of 500 mating cycles while meeting the performance criteria as specified in Performance Groups D and F in Section 7.11

7.7 Plug Connector

Figure 7.6 provides basic dimensional information for the mating interface of the P&D-D plug connector. The plug connector is defined as the connector with exposed male contacts.

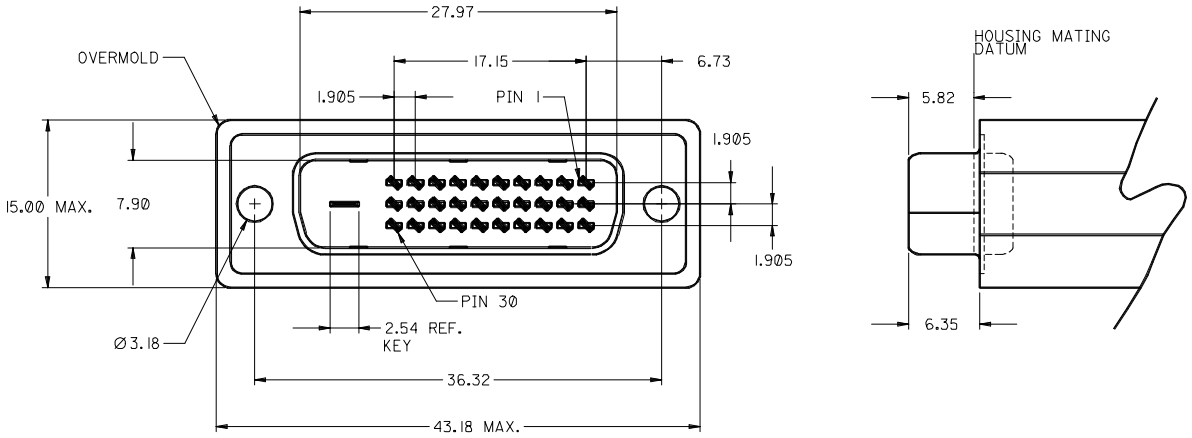


Figure 7-6 : P&D-D Plug Connector - Basic Mating Interface Dimensions

Notes:
1. Dimensions are in mm.
2. Dimensions and tolerances per ASME Y14.5M - 1994
3. Illustrations are in third angle projection
4. Not to scale

7.7.1 Plug Connector Termination

The termination of the wire to the plug contacts may be varied to suit the manufacturing process needs of the cable assembler while meeting the requirements of section 7.10. For reference, the following methods are listed: crimp, insulation displacement (IDC), insulation piercing, welding, and soldering.

7.8 Pinouts

The signals supported by the P&D-A/D and P&D-D will be provided on the connector as follows:

P&D-A/D	P&D-D
Analogue Video	
Charging Power	Charging Power
TMDS Digital Video	TMDS Digital Video
Display Data Channel (DDC2)	Display Data Channel (DDC2)
Hz. And Vt. Sync. [1]	
IEEE 1394	IEEE 1394
Pixel Clock	
Stereo sync. [1]	
Universal Serial Bus (USB)	Universal Serial Bus (USB)

Table 7-1 : P&D-A/D and P&D-D Signals

[1] Hz., Vt. And Stereo sync. pulses will be carried on the TMDS interface if used, else may be carried on dedicated pins.

7.8.1 Contact Sequencing

Tables 7.2 and 7.3 describe pin sequencing and their location per figures 7.1 and 7.3.

Pin	Function	Pin	Function
1	General Purpose, Third Make	18	General Purpose, Fourth Make
2	General Purpose, Third Make	19	General Purpose, Third Make
3	General Purpose, Third Make	20	General Purpose, Third Make
4	General Purpose, Third Make	21	General Purpose, Third Make
5	General Purpose, Third Make	22	General Purpose, Third Make
6	General Purpose, Third Make	23	General Purpose, Third Make
7	General Purpose, Third Make	24	General Purpose, Third Make
8	General Purpose, Fourth Make	25	General Purpose, Third Make
9	General Purpose, Third Make	26	General Purpose, Third Make
10	General Purpose, Third Make	27	General Purpose, Third Make
11	General Purpose, Third Make	28	General Purpose, Fourth Make
12	General Purpose, Third Make	29	General Purpose, Third Make
13	General Purpose, Third Make	30	General Purpose, Third Make
14	General Purpose, Third Make	C1	Quasi-Coaxial, Fourth Make
15	General Purpose, Third Make	C2	Quasi-Coaxial, Fourth Make
16	General Purpose, Third Make	C3	Quasi-Coaxial, Fourth Make
17	General Purpose, Third Make	C4	Quasi-Coaxial, Fourth Make
		C5	Common Ground for Quasi Coaxial Lines, Second Make
Shell	First Make		

Table 7-2 : Contact Sequencing

7.8.2 P&D-A/D Signal Pin Assignments - Main Pin Field

Pin	Signal	Pin	Signal
1	TMDS Data2 +	16	USB data +
2	TMDS Data2 -	17	USB data -
3	TMDS Data2 return	18	1394 outer shield (optional) & Charge Power return[2]
4	Hz. and Vt. Sync. return	19	1394 Vg
5	Horizontal Sync. / Composite Sync.	20	1394 Vp
6	Vertical Sync.	21	TMDS Data0 +
7	TMDS Clock return	22	TMDS Data0 -
8	Charge power + [1]	23	TMDS Data0 return
9	1394 pair A, data -	24	Stereo sync.
10	1394 pair A, data +	25	DDC return & Stereo Sync. Return
11	TMDS Data1 +	26	DDC data (SDA)
12	TMDS Data1 -	27	DDC clock (SCL)
13	TMDS Data1 return	28	+5 VDC
14	TMDS Clock +	29	1394 pair B, Clock +
15	TMDS Clock -	30	1394 pair B, Clock -

Table 7-3 : P&D-A/D Signal Assignment - Main Pin Field

[1] Optional output from monitor, see section 4.6 for details.

[2] Note: The IEEE-1394 internal cable bundle may need an outer shield to minimise internal crosstalk within the cable construction. The outer EMI containment shield for the IEEE-1394 function will be provided by the overall P&D cable shield. If the internal bundle shield for IEEE-1394 is required this may be terminated to pin #18. It is recommended that this implementation be evaluated in the case where both Charge Power return and the IEEE-1394 internal cable bundle shield will be commoned to pin #18.

7.8.3 Signal Pin Assignments - MicroCross™ Section

Pin	Signal
C1	Red Video Out
C2	Green Video Out
C3	Pixel clock (optional)
C4	Blue Video Out
C5[1]	Video / Pixel Clock Return

Table 7-4 : Signal Assignment - MicroCross™ Section

[1] C5 designates the shield cross at the center of pins C1, C2, C3 and C4.

7.8.4 P&D-D Signal Pin Assignments - Pin Field

Pin	Signal	Pin	Signal
1	TMDS Data2 +	16	USB data +
2	TMDS Data2 -	17	USB data -
3	TMDS Data2 return	18	1394 outer shield (optional) & Charge Power return[2]
4	Unused	19	1394 Vg
5	Unused	20	1394 Vp
6	Unused	21	TMDS Data0 +
7	TMDS Clock return	22	TMDS Data0 -
8	Charge power + [1]	23	TMDS Data0 return
9	1394 pair A, data -	24	Unused
10	1394 pair A, data +	25	DDC return
11	TMDS Data1 +	26	DDC data (SDA)
12	TMDS Data1 -	27	DDC clock (SCL)
13	TMDS Data1 return	28	+5 VDC
14	TMDS Clock +	29	1394 pair B, Clock +
15	TMDS Clock -	30	1394 pair B, Clock -

Table 7-5 : Signal Assignment - Main Pin Field

[1] Optional output from monitor, see section 4.6 for details.

[2] Note: The IEEE-1394 internal cable bundle may need an outer shield to minimise internal crosstalk within the cable construction. The outer EMI containment shield for the IEEE-1394 function will be provided by the overall P&D cable shield. If the internal bundle shield for IEEE-1394 is required this may be terminated to pin #18. It is recommended that this implementation be evaluated in the case where both Charge Power return and the IEEE-1394 internal cable bundle shield will be commoned to pin #18.

7.9 Connector Performance Characteristics

This section summarises the Environmental, Electrical, and Mechanical Performance Characteristics of the P&D connector. ANSI/EIA-364 Test Procedures and Conditions, or requirements are noted where applicable. Details of the Connector Performance test criteria and groups with test sequences may be found in Section 7.10.

7.9.1 Environmental

7.9.1.1 Thermal Shock

Conditions: ANSI/EIA-364-32, Condition 1
10 Cycles, mated/unmated

7.9.1.2 Cyclic Humidity

Conditions: ANSI/EIA-364-31, Condition A, C
Method III, omit 7A and 7B

7.9.1.3 Temperature Life

Conditions: ANSI/EIA-364-17, Condition 4
105° C for 250 hours
Method A, mated

7.9.1.4 Corrosion Resistance

Conditions: ANSI/EIA-364-65, Environmental Class II
Locate sample in zone 14

7.9.2 Electrical

7.9.2.1 Contact Resistance

Conditions: ANSI/EIA-364-23
15 mΩ, maximum, initial per contact mated pair
10 mΩ, maximum change from original per contact mated pair

7.9.2.2 Dielectric Withstanding Voltage

Conditions: ANSI/EIA-364-20
Test voltage 500V DC +/- 50 V
Method C, unmated and unmounted
Barometric pressure of 15psi

7.9.2.3 Insulation Resistance

Conditions: ANSI/EIA-364-21
Test voltage 500V DC +/- 50 V
Method C, unmated and unmounted

7.9.2.4 Shell-to-Shell and Shell-to-Bulkhead Resistance

Conditions: VP&D appendix E, section 14.2
50mΩ, maximum, initial
50mΩ, maximum change from original

7.9.2.5 Contact Current Rating

Conditions: ANSI/EIA-364-70, TP-70
55 °C, maximum ambient
85 °C, maximum temperature change
1.5A minimum

7.9.2.6 Impedance: General Purpose Lines

Conditions: ANSI/EIA-364-67[1]
TDR method normalised to 1ns risetime, single ended
1:1 S:G ratio
55Ω to 75Ω

7.9.2.7 Impedance: Differential Lines

Conditions: ANSI/EIA-364-67[1]
TDR method normalised to 500ps risetime
Shell only grounded
Z_{SOURCE} & Z_{LOAD} = 105Ω
105Ω +/- 10%

7.9.2.8 Impedance: Quasi-Coaxial Lines

Conditions: ANSI/EIA-364-67[1]
TDR method normalised to 1ns risetime
75Ω +/- 10%

7.9.2.9 Bandwidth: General Purpose Lines - Single Ended

Conditions: See appendix E, section 14
Calculation based on risetime measurement, single ended
1:1 S:G ratio
0.8 GHz minimum

7.9.2.10 Bandwidth: General Purpose Lines - Differential

Conditions: See appendix E, section 14
Calculation based on risetime measurement, differential
1:1 S:G ratio
2.4 GHz minimum

7.9.2.11 Bandwidth: Quasi-Coaxial Lines

Conditions: See appendix E, section 14
Calculation based on risetime measurement
2.4 GHz minimum

7.9.2.12 Crosstalk: General Purpose - Differential

Conditions: ANSI/EIA-364-90 [1]
1V / 500ps, Measure NEXT & FEXT
Shield only grounded
5% maximum

7.9.2.13 Crosstalk: Quasi-Coaxial Lines

Conditions: ANSI/EIA-364-90 [1]
1V / 1ns, Measure NEXT & FEXT
5% maximum

[1] At time of preparation of this standard, ANSI/EIA-364-67 and ANSI/EIA-34-90 have not been ratified and are cited as the recommended test procedures. The impedance values are described in ohms as calculated from the "% reflection" as specified in ANSI/EIA-364-67.

7.9.3 Mechanical

7.9.3.1 Vibration

Conditions: ANSI/EIA-364-28, Condition III

7.9.3.2 Mechanical Shock

Conditions: ANSI/EIA-364-27 Condition G

7.9.3.3 Durability

Conditions: ANSI/EIA-364-09
2 mated pairs, 5 cycles
2 mated pairs, Automatic cycling to 500 cycles
Rate: 500 +/- 50 cycles/hour

7.9.3.4 Mating and Unmating Forces

Conditions: ANSI/EIA-364-13
Insert and extract at speed of 25mm / minute
Unmating force: 1 kgf minimum, 4 kgf maximum

7.10 Connector Performance Test Criteria

To verify the performance requirements, performance testing is specified according to the recommendations, test sequences and test procedures of ANSI/EIA-364, entitled “Electrical Connector Test Procedures Including Environmental Classifications”. Table 1 of ANSI/EIA-364 shows operating class definitions for different end-use applications. For the VESA P&D connector, the test specifications follow the recommendations for environmental class 1.3, which is defined as follows: “ No air conditioning of humidity control with normal heating and ventilation”.
The Equipment operating Environmental Conditions shown, for class 1.3 in Table 2 are:

- Temperature: +15° C to +85° C
- Humidity: 95% maximum.

Class 1.3 is further described as operating in a “harsh environmental” state, but with no marine atmosphere.

Accordingly, the performance groupings, sequences within each group, and the test procedures will follow the recommendations of ANSI/EIA-364, except where the unique requirements of the P&D connector and cable assembly may call for tests which are not covered in ANSI/EIA-364, or where the requirements deviate substantially from those in that document. In those cases, test procedures of other recognised authorities or specific procedures described in the annexes will be cited.

Receptacles, plugs and cable terminations shall perform to the requirements and pass all the following tests in the groups and sequences shown.

Testing may be done as follows:

a) Plug and receptacle only.
In this case, for those performance groups that require it, the plugs may be assembled to the cable to provide a cable assembly.

b) Cable assembly (with a plug on each end) and receptacle.
In this case, performance testing for both elements may be combined.

c) Cable assembly only (with a plug on each end).
In this case, the cable assembly supplier should use a plug connector source which has successfully passed performance testing, according to this standard.

d) Plug only, or receptacle only.
In this case, the other half shall be procured from a source, which has successfully passed performance testing, according to this standard. For those performance groups that require it, the plugs may be assembled to the cable to provide a cable assembly.

All resistance values shown in the following performance groups are for connectors only, including their terminations to the wire and/or PC board, but excluding the resistance of the wire. Resistance measurements shall be performed in an environment of temperature, pressure and humidity specified by ANSI/EIA-364.

The numbers of units to be tested is a recommended minimum; the actual sample size is to be determined by requirements of users.

7.10.1 Connector Performance Test Groups

7.10.1.1 Performance group A: Basic mechanical and dimensional conformance & electrical functionality when subjected to mechanical shock & vibration

Number of samples:

[2] Receptacles, unassembled to PCB used for Phase 1, A1 and A2 (one each)
[2] Receptacles, assembled to PCB
[2] Plugs, unassembled to cable used for Phase 1, A1 and A2 (one each)
[2] Cable assemblies with a plug assembled to one end, 25.4 cm long.

	Test			**Measurements to be performed**		**Requirements**
Phase	**Title**	**ID No.**	**Severity or conditions**	**Title**	**ID No.**	**Performance Level**
A1	Visual and dimensional inspection	ANSI/EIA 364-18	Unmated connectors	Dimensional inspection		
A2	Plating thickness measure-ments					Record thicknesses; see clause 2.1.2
A3	None			Low level contact resistance	ANSI/EIA 364-23	15 mΩ, maximum, initial per contact mated pair. (Each contact)
A4	Vibration	ANSI/EIA 364-28	Method 5A, 15 min/axis	Continuity	ANSI/EIA 364-46	No discontinuity at 1 μs or longer. (Each contact)
A5	None			Low level contact resistance	ANSI/EIA 364-23	10 mΩ maximum change from original per contact mated pair. (Each contact)
A6	Mechanical shock (specified pulse)	ANSI/EIA 364-27	Condition A see note 1	Continuity	ANSI/EIA 364-46	No discontinuity at 1 μs or longer. (Each contact)
A7	None			Low level contact resistance.	ANSI/EIA 364-23	15 mΩ maximum change from original per contact mated pair. (Each contact)

Table 7-6 : Performance Group A

Note 1: Connectors are to be mounted on a fixture which simulates typical usage. The socket shall be mounted to a panel which is permanently affixed to the fixture. The mounting means shall include typical accessories such as:

1. An insulating member to prevent grounding of the shell to the panel
2. A PCB in accord with the pattern shown in Figure 7.5 for the receptacle being tested. The PCB shall also be permanently affixed to the fixture.

The plug shall be mated with the receptacle, and the other end of the cable shall be permanently clamped to the fixture.

7.10.1.2 Performance Group B: Low level contact resistance when subjected to thermal shock & humidity stress

Number of samples:

[2] Receptacles, assembled to PCB

[2] Cable assemblies with a plug assembled to one end, 25.4 cm. long

	Test			**Measurements to be performed**		**Requirements**
Phase	**Title**	**ID No.**	**Severity or conditions**	**Title**	**ID No.**	**Performance Level**
B1	None			Low level contact resistance	ANSI/EIA 364-23	15 mΩ maximum, initial per contact mated pair. (Each contact)
B2	Thermal shock	ANSI/EIA 364-32	Condition I 10 cycles (mated)	Low level contact resistance	ANSI/EIA 364-23	10 mΩ maximum change from initial per contact mated pair. (All samples to be mated)
B3	Humidity	ANSI/EIA 364-31	Condition C (504 hrs.) Method III (cycling) non-energized. Omit 7a & 7b (mated)	Low level contact resistance	ANSI/EIA 364-23	10 mΩ maximum change from initial per contact mated pair. (All samples to be mated)

Table 7-7 : Performance Group B

7.10.1.3 Performance Group C: Low level contact resistance when subjected to thermal shock & humidity stress

Number of samples:

[2] Receptacles, assembled to PCB

[2] Cable assemblies with a plug assembled to one end, 2 m. long

	Test			Measurements to be performed		Requirements
Phase	Title	ID No.	Severity or conditions	Title	ID No.	Performance Level
C1	Withstanding voltage	ANSI/EIA 364-20	Test voltage 500 VDC +50/-50 V Method C (unmated and unmounted)	Withstanding voltage	ANSI/EIA 364-20	No flashover. No sparkover. No excess leakage. No breakdown.
C2	Thermal shock	ANSI/EIA 364-32	Condition I 10 cycles (unmated)	Withstanding voltage (same conditions as C1)	ANSI/EIA 364-20	No flashover. No sparkover. No excess leakage. No breakdown.
C3	Insulation resistance	ANSI/EIA 364-21	Test voltage 500 VDC +50/-50 V (unmated and unmounted)	Insulation resistance	ANSI/EIA 364-21	1 GΩ minimum, between adjacent contacts and contacts and shell
C4	Humidity (cyclic)	ANSI/EIA 364-31	Condition A (96 hrs.) Method III non-energized. Omit steps 7a and 7b	Insulation resistance (same conditions as C3)	ANSI/EIA 364-21	1 GΩ minimum.

Table 7-8 : Performance Group C

7.10.1.4 Performance Group D: Contact life & durability when subjected to mechanical cycling & corrosive gas exposure

Number of samples:

[2] Receptacles, assembled to PCB

[2] Cable assemblies with a plug assembled to one end, 25.4 cm. Long.

	Test			Measurements to be performed		Requirements
Phase	Title	ID No.	Severity or Conditions	Title	ID No.	Performance Level
D1	None			Low level contact resistance	ANSI/EIA 364-23	15 mΩ maximum, initial per contact pair. (Each contact)
D2	Continuity housing (shell)			Contact resistance, braid to receptacle shell	ANSI/EIA 364-06	50 mΩ maximum, initial from braid to receptacle shell at 100 mA, 5VDC open circuit max.
D3	Durability	ANSI/EIA 364-09	(a) 2 mated pairs, 5 cycles (b) 2 mated pairs, automatic cycling to 250 cycles, rate 500 cycles/hr +10/-10 cycles			
D4	None			Low level contact resistance	ANSI/EIA 364-23	10 mΩ maximum change per contact pair. (Each contact)
D5	Continuity Housing (shell)			Contact resistance	ANSI/EIA 364-06	50 mΩ maximum, change from initial from braid to receptacle shell at 100 mA, 5VDC open circuit max.
D6	Mixed flowing gas (in unmated condition)	ANSI/EIA 364-65	Class II exposures: (a) 2 mated pairs-unmated for 1 day (b) 2 mated pairs-mated 10 days	Low level contact resistance	ANSI/EIA 364-23	10 mΩ maximum change from original per contact pair. (Each contact). Measured at end of exposure.
D7	Durability	ANSI/EIA 364-09	Class II exposures: (a) 2 mated pairs, 5 cycles (b) 2 mated pairs, automatic cycling to 250 cycles, rate 500 cycles/hr +/- 10 cycles			
D8	Mixed flowing gas (in mated condition)	ANSI/EIA 364-65	Class II Exposures: Expose mated for 10 days	Low level contact resistance at end of exposure	ANSI/EIA 364-23	10 mΩ maximum change from original per contact pair. (Each contact). Measured at end of exposure.
D9	Continuity housing (shell)			Contact resistance	ANSI/EIA 364-06	50 mΩ maximum, initial from braid to receptacle shell at 100 mA, 5VDC open circuit max.

Table 7-9 : Performance Group D

7.10.1.5 Performance Group E: Contact resistance & unmating force when subjected to temperature life stress

Number of samples:

[2] Receptacles, assembled to PCB

[2] Cable assemblies with a plug assembled to one end, 2m long.

	Test			Measurements to be performed		Requirements
Phase	Title	ID No.	Severity or conditions	Title	ID No.	Performance Level
E1	Unmating forces	ANSI/EIA 364-13	Mount socket rigidly, insert receptacle by hand Auto Rate: 25 mm/min.	Unmating only	ANSI/EIA 364-13	Unmating force: 1 kgf minimum 4 kgf maximum
E2	None			Low level contact resistance	ANSI/EIA 364-23	15 mΩ maximum, initial per contact pair. (All contacts in 2 connectors.)
E3	Continuity - housing (shell)			Contact resistance	ANSI/EIA 364-06	50 mΩ maximum, initial from braid to receptacle shell at 100 mA, 5VDC open circuit max.
E4	Temperature life	ANSI/EIA 364-17	Condition 4 (105° C) 250 hrs. Method A (mated)	Low level contact resistance	ANSI/EIA 364-23	10 mΩ maximum change per contact pair. (All contacts in 2 connectors)
E5	Continuity housing (shell)			Contact resistance	ANSI/EIA 364-06	50 mΩ maximum, change from initial from braid to receptacle shell at 100 mA, 5VDC open circuit max.
E6	Unmating forces	ANSI/EIA 364-13	Mount socket rigidly. Insert plug by hand. Auto Rate: 25mm/min.	Unmating only	ANSI/EIA 364-13	Unmating force: 1 kgf minimum, 4 kgf maximum

Table 7-10 : Performance Group E

7.10.1.6 Performance Group F: Mechanical retention and durability

Number of samples:

[2] Receptacles, assembled to PCB

[2] Plugs assembled to cable, one end only, 25.4 cm long.

	Test			Measurements to be performed		Requirements
Phase	Title	ID No.	Severity or conditions	Title	ID No.	Performance Level
F1	Mating and unmating forces	ANSI/EIA 364-13	Auto Rate: 25mm/min.	Unmating only	ANSI/EIA 364-13	Unmating force: 1kgf minimum, 4 kgf maximum
F2	Durability	ANSI/EIA 364-09 500 cycles/hr +/- 50 cycles	Automatic cycling to 500 cycles	Unmating only	ANSI/EIA 364-13	Unmating force at end of durability cycles: 1kgf minimum, 4 kgf maximum.

Table 7-11 : Performance Group F

7.10.1.7 Performance Group FP: Electrical Test - General Purpose Line, Single Ended

Number of samples:

[2] Receptacles, assembled to PCB
[2] Plugs terminated to PCB

	Test			Measurements to be performed		Requirements
Phase	Title	ID No.	Severity or conditions	Title	ID No.	Performance Level
FP5	Impedance Single Ended	EIA 364-67 [1]	TDR method, normalized to 1 ns, single ended 1:1 S:G ratio	Time domain reflecto-meter	EIA 364-67[1]	55 to 75 Ω
FP6	Bandwidth Single Ended	See note[e2]	single ended 1:1 S:G ratio	Measure t rise Calculate BW	See note [2]	0.8 GHz Min.

Table 7-12 : Performance group FP - General Purpose, Single Ended

Notes: This chart applies only to the thirty general purpose lines.

[1] At time of preparation of this standard, ANSI/EIA-364-67 had not been ratified and is cited as a recommended test procedure.

[2] No current test appendix exists in ANSI/EIA-364 for Bandwidth testing, see appendix E, section 14 for reference test procedure.

7.10.1.8 Performance Group FP: Electrical Test - General Purpose Lines, Differential

Number of samples:

[2] Receptacles, assembled to PCB
[2] Plugs terminated to PCB

	Test			Measurements to be performed		Requirements
Phase	Title	ID No.	Severity or conditions	Title	ID No.	Performance Level
FP4	Crosstalk Differential	EIA 364-90 [1]	1 V/500ps Shell only grounded	Measure NEXT & FEXT	EIA 364-90 [1]	5 % Max.
FP5	Impedance Differential	EIA 364-67 [1]	Differential TDR method normalized to 500 ps Shell only grounded Z_{SOURCE} & Z_{LOAD} = 105Ω	Time domain reflecto-meter	EIA 364-67 [1]	105Ω +/- 10%
FP6	Bandwidth Differential	See note [2]	1:1 S:G environment	Measure t rise Calculate BW	See note [2]	2.4 GHz Min.

Table 7-13 : Performance Group FP - General Purpose, Differential

Notes: This chart applies only to the thirty general purpose lines.

[1] At time of preparation of this standard, ANSI/EIA-364-67 and ANSI/EIA-364-90 have not been ratified and are cited as recommended test procedures.

[2] No current test appendix exists in ANSI/EIA-364 for Bandwidth testing, see appendix E, section 14 for reference test procedure.

7.10.1.9 Performance Group FP: Electrical Tests - Quasi-coaxial Lines

Number of samples:

[2] Receptacles, assembled to PCB
[2] Plugs terminated to 76.2mm (typ.) of semi-rigid 75Ω cable.

	Test			Measurements to be performed		Requirements
Phase	Title	ID No.	Severity or conditions	Title	ID No.	Performance Level
FP4	Crosstalk	EIA 364-90[1]	1 V/ 1 ns	Measure NEXT & FEXT	EIA 364-90[1]	5% Max.
FP5	Impedance	EIA 364-67[1]	TDR method, normalized to 1 ns	Time domain reflecto-meter	EIA 364-67[1]	75Ω +/- 10%
FP6	Bandwidth	See note [2]		Measure t rise Calculate BW	See note [2]	2.4 GHz Min.

Table 7-14 : Performance Group FP - Quasi-coaxial Lines

Notes: This chart applies only to the four Quasi-coaxial lines.

[1] At time of preparation of this standard, ANSI/EIA-364-67 and ANSI/EIA-364-90 have not been ratified and are cited as recommended test procedures.

[2] No current test appendix exists in ANSI/EIA-364 for Bandwidth testing, see appendix E, section 14 for reference test procedure.

7.10.1.10 Performance Group G: General tests

Suggested procedures to test miscellaneous but important aspects of the interconnect.

Since the tests listed below may be destructive, separate samples must be used for each test. The number of samples to be used is listed under the test title.

	Test			Measurements to be performed		Requirements
Phase	Title	ID No.	Severity or conditions	Title	ID No.	Performance Level
G1	Electrostatic discharge	IEC 801-2	1 to 8 kV in 1 kV steps. Use 8 mm ball probe. Test unmated	Evidence of discharge		No evidence of discharge to any of the 34 contacts; discharge to shield is acceptable.
G2	Cable flexing [2 plugs]	ANSI/EIA 364-41	Condition I, dimension X=3.7x cable diameter; 100 cycles in each of two planes	Withstanding voltage	per C1	per C1
				Insulation resistance	per C3	per C3
				Continuity	ANSI/EIA 364-46	No discontinuity on contacts or shield greater than 1 μs during flexing.

Table 7-15 : Performance Group G

8. Physical Layer: Cable Assembly Specifications

Cable assembly specification has a "Type x" designation where 'x' is a alphanumeric code. These type designations are a cross reference to the VESA P&D Architecture Document.

These requirements apply to cable assemblies regardless of length.

Type Designation	Corresponding Sublayer
A	Analogue Video
AT/AT'	TMDS Video
C	Sync and DDC
D	Charging Power and +5 VDC
USB	USB
1394	1394

Table 8-1 : Physical Sublayer Designations

8.1 TMDS Video Sublayer, Type AT/AT'

Parameter	Value	Conditions
Impedance	100 +/- 5Ω	
Time Delay Skew	300 ps max. within a pair	65 MHz
	1300 ps max. Between pairs	65 MHz
	180ps max. within a pair	112 MHz
	750ps max. between pairs	112 MHhz Ref. Section 6.4.1 (T_{CKJ})
Conductor DC Resistance	3.6Ω max.	At 20° C
Near End Crosstalk	3.8% max. Between any 2 pairs	Drive waveform is a 300ps rise time (20% - 80%) pulse
Far End Crosstalk	1.0% max. between any 2 pairs	Drive waveform is a 300ps rise time (20% - 80%) pulse.

Table 8-2 : TMDS Video Sublayer Attributes (part 1)

Attenuation		
Frequency (MHz)	**65 MHz TMDS**	**112 MHz TMDS**
1	0.55 dB max.	0.40 dB max.
10	1.3 dB max.	0.88 dB max.
50	2.3 dB max.	1.7 dB max.
100	3.1 dB max.	2.2 dB max.
200	4.4 dB max.	3.2 dB max.
400	6.0 dB max.	4.6 dB max.
600	8.2 dB max.	5.9 dB max.

Table 8-3 : TMDS Video sublayer attributes (part 2)

8.2 Analogue Video Sublayer (Coax), Type A

Parameter	Value	Conditions
Impedance	75Ω +/- 4Ω	
Conductor DC Resistance	1.8Ω max.	At 20° C

Table 8-4 : Analogue Video Sublayer Attributes # 1

Attenuation	
Frequency (MHz)	
1	0.14 dB max.
10	0.45 dB max.
50	1.0 dB max.
100	1.5 dB max.
200	2.1 dB max.
400	3.0 dB max.
700	4.3 dB max.
1000	5.4 dB max.

Table 8-5 : Analogue Video Sublayer Attributes # 2

8.3 Conductors for Vertical, Horizontal, Stereo Sync., Sync. Return and DDC, Type C

Conductor DC resistance: 3.6Ω maximum at 20° C

8.4 Conductors for Charge Power and +5VDC, Type D

Conductor DC resistance: 2.3Ω maximum at 20° C
Current carrying capacity: 1.5A minimum

8.5 USB Sublayer, Type USB

Electrical performance requirements shall be per the Universal Serial Bus specification.

8.6 IEEE 1394-1995 Sublayer, Type 1394

Electrical performance requirements shall be per IEEE-1394-1995 specification.

8.7 Cable Type Usage : P&D-A/D

Cable Type	Pin	Signal	Cable Type	Pin	Signal
AT	1	TMDS Data2 +	1394	19	1394 Vg
AT’	2	TMDS Data2 -	1394	20	1394 Vp
AT/AT’	3	TMDS Data2 return	AT	21	TMDS Data0 +
C	4	Hz. & Vt. Sync. return	AT’	22	TMDS Data0 -
C	5	Horizontal Sync. / Composite Sync.	AT/AT’	23	TMDS Data0 return
C	6	Vertical Sync.	C	24	Stereo sync.
AT/AT’	7	TMDS Clock return	C	25	DDC return & Stereo Sync. return
D	8	Charge power + [1]	C	26	DDC data (SDA)
1394	9	1394 pair A, data -	C	27	DDC clock (SCL)
1394	10	1394 pair A, data +	C	28	+5 VDC
AT	11	TMDS Data1 +	1394	29	1394 pair B, clock +
AT’	12	TMDS Data1 -	1394	30	1394 pair B, clock -
AT/AT’	13	TMDS Data1 return	A	C1	Red Video Out
AT	14	TMDS Clock +	A	C2	Green Video Out
AT’	15	TMDS Clock -	A	C3	Pixel Clock (optional)
USB	16	USB data +	A	C4	Blue Video Out
USB	17	USB data -	A	C5	Video / Pixel Clock return
D + 1394	18	1394 shield (optional) & Charge power return[2]			

Table 8-6 : Cable Type Usage - P&D-A/D

[1] Optional output from monitor, see section 4.6 for details.

[2] Note: The IEEE-1394 internal cable bundle may need an outer shield to minimise internal crosstalk within the cable construction. The outer EMI containment shield for the IEEE-1394 function will be provided by the overall P&D cable shield. If the internal bundle shield for IEEE-1394 is required this may be terminated to pin #18. It is recommended that this implementation be evaluated in the case where both Charge Power return and the IEEE-1394 internal cable bundle shield will be commoned to pin #18.

8.8 Cable Type Usage : P&D-D

Cable Type	Pin	Signal	Cable Type	Pin	Signal
AT	1	TMDS Data2 +	1394	19	1394 Vg
AT’	2	TMDS Data2 -	1394	20	1394 Vp
AT/AT’	3	TMDS Data2 return	AT	21	TMDS Data0 +
	4	Unused	AT’	22	TMDS Data0 -
	5	Unused	AT/AT’	23	TMDS Data0 return
	6	Unused		24	Unused
AT/AT’	7	TMDS Clock return	C	25	DDC return
D	8	Charge power +	C	26	DDC data (SDA)
1394	9	1394 pair A, data -	C	27	DDC clock (SCL)
1394	10	1394 pair A, data +	C	28	+5 VDC
AT	11	TMDS Data1 +	1394	29	1394 pair B, clock +
AT’	12	TMDS Data1 -	1394	30	1394 pair B, clock -
AT/AT’	13	TMDS Data1 return			
AT	14	TMDS Clock +			
AT’	15	TMDS Clock -			
USB	16	USB data +			
USB	17	USB data -			
D + 1394	18	1394 shield & Charge power return			

Table 8-7 : Cable Type Usage - P&D-D

9. Compliance with Plug and Display Standard

This section defines the requirements for any piece of hardware (e.g. host system, graphic card, display) to be able to claim that it is compliant with the VESA Plug and Display Standard.

9.1 A P&D-A/D Compliant Host System / Graphic Card / etc.

A P&D-A/D compliant host system, graphic card (or similar) must have the following attributes:

1. DDC2 capability
2. Capability to decode and use the EDID Version 3 structure
3. A P&D-A/D receptacle
4. The P&D TMDS interface
5. An analogue interface (R/G/B and 2 syncs. or R/G/B and composite sync.)
6. Support for hot-plugging protection (see Section 3)
7. It may also contain any or all of the following:
    - IEEE-1394-1995
    - USB
    - Pixel clock
    - Stereo sync.
    - Provision to use charge power

9.2 A P&D-D Compliant Host System / Graphic Card / etc.

A P&D-D compliant host system, graphic card (or similar) must have the following attributes:

1. DDC2 capability
2. Capability to decode and use the EDID Version 3 structure
3. A P&D-D receptacle
4. The P&D TMDS interface
5. Support for hot-plugging protection (see Section 3)
6. It may also contain any or all of the following:
    - IEEE-1394-1995
    - USB
    - Provision to use charge power

9.3 A P&D Compliant Display

A P&D compliant display must have the following attributes:

1. DDC2 capability
2. Capability to send the appropriate EDID Version 3 structure
3. A P&D plug
4. The P&D-D TMDS interface
5. Support for hot-plugging protection (see Section 3)
6. It may also contain any or all of the following:
    - IEEE-1394-1995
    - USB
    - Stereo sync. (carried via TMDS)
    - Provision to supply charge power
7. The capability to indicate to the user if the host system does not respond with the EDID requested video data stream

9.4 P&D Symbol

It is required that the following symbol be used on system units adjacent to the P&D receptacle and on the P&D plug on the end of the video cable intended to plug into the system unit - this will give end users a clear indication of which interface options are supported.

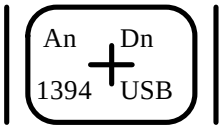


Figure 9-1 : P&D Symbol

Following expands the definition of each quadrant. If no support is provided for a feature then the corresponding quadrant shall be left blank.

9.4.1 Upper Left Quadrant

Defines the analogue interface support:

A1 : RS-170
A2 : RS-343
A3 : Euro
A4 : VESA

9.4.2 Upper Right Quadrant

Defines the TMDS operating range:

D : Operating range is non-standard (at time of writing)
D1 : range of 25 ⇒ 65 MHz
D2 : range of 65 ⇒ 112 MHz
D3 : range of 112 ⇒ 160 MHz

9.4.3 Lower Left Quadrant

Indicates support for IEEE 1394-1995

9.4.4 Lower Right Quadrant

Indicates support for USB

9.4.5 Example

A system supporting analogue video in VESA format, TMDS with 25 ⇒ 65 MHz operating range, IEEE 1394-1995 and USB would use one of these symbols:

Figure 9-2 : P&D Symbol Example

9.4.6 Additional Information

If TMDS does not operate over one of the predefined ranges then it is recommended that the actual operating range be printed on the cable with the upper right quadrant carrying the letter ‘D’ only.

The following sections of this standard are informative appendices and do not constitute part of the VESA Plug and Display Standard.

10. Appendix A: Digital Monitor Cable Assembly

This is an informative appendix and does not form part of the VESA Plug and Display Standard.

10.1 Introduction

Two configurations are recommended for digital only interface implementations using detachable signal cables, benefits include:

- Standard cable assembly
    - Shorter lead time
    - Lower cost
        - No unique cables
        - Lower inventory level
- Multiple suppliers

Different cable lengths and configurations are possible e.g. 5m and 10m

- Minimum configuration: DDC2 + TMDS channel
- Maximum configuration: DDC2 + TMDS + USB + IEEE 1394 + Charge Power

Notes:

1. The USB and IEEE 1394-1995 specifications have cable length constraints, check the appropriate specification for details.
2. It is important to ensure that the connector and cable components and construction techniques used result in an assembly that meets the performance requirements defined in this standard.
   In particular, an appropriate cable termination technique should be used at the 40 pin microribbon.

10.2 P&D-D ⇔ P&D-D Plug Connectors

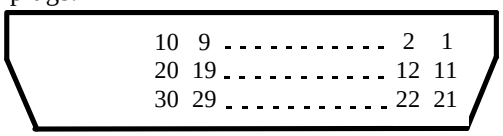
A cable using P&D-D plug connectors on both ends with a 1:1 pin relationship as shown is Table 10.1 is acceptable.

10.2.1 Pin Definitions

Pin	P&D-D Connector Main Field	Pin	P&D-D Connector Main Field
1	TMDS Data2 +	1	TMDS Data2 +
2	TMDS Data2 -	2	TMDS Data2 -
3	TMDS Data2 return	3	TMDS Data2 return
4	Unused	4	Unused
5	Unused	5	Unused
6	Unused	6	Unused
7	TMDS Clock return	7	TMDS Clock return
8	Charge power +	8	Charge power +
9	1394 pair A, data -	9	1394 pair A, data -
10	1394 pair A, data +	10	1394 pair A, data +
11	TMDS Data1 +	11	TMDS Data1 +
12	TMDS Data1 -	12	TMDS Data1 -
13	TMDS Data1 return	13	TMDS Data1 return
14	TMDS Clock +	14	TMDS Clock +
15	TMDS Clock -	15	TMDS Clock -
16	USB data +	16	USB data +
17	USB data -	17	USB data -
18	1394 outer shield (optional) & Charge power return	18	1394 outer shield (optional) & Charge power return
19	1394 Vg	19	1394 Vg
20	1394 Vp	20	1394 Vp
21	TMDS Data0 +	21	TMDS Data0 +
22	TMDS Data0 -	22	TMDS Data0 -
23	TMDS Data0 return	23	TMDS Data0 return
24	Unused	24	Unused
25	DDC return	25	DDC return
26	DDC data (SDA)	26	DDC data (SDA)
27	DDC clock (SCL)	27	DDC clock (SCL)
28	+5V dc	28	+5V dc
29	1394 pair B, clock+	29	1394 pair B, clock+
30	1394 pair B, clock -	30	1394 pair B, clock -

Figure 10-1 : Pin Definitions, P&D-D ⇔ P&D-D

Numbering convention on P&D-D plugs:



10.3 P&D-D ⇔ Microribbon Plug Connector

10.3.1 Assembly Drawing

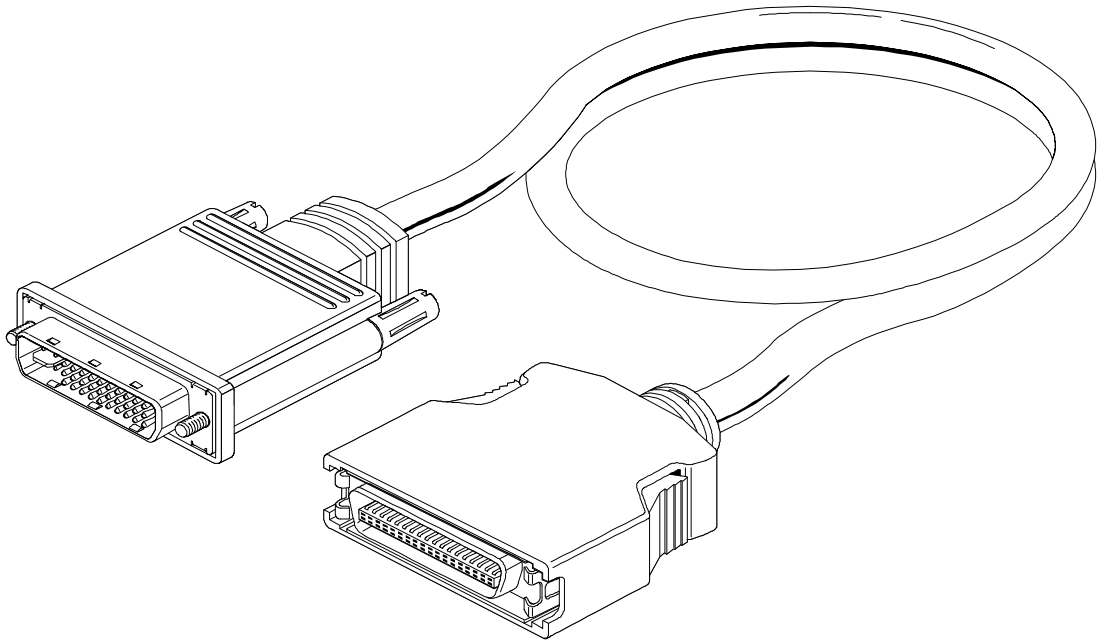


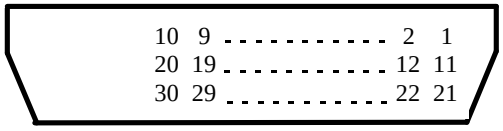
Figure 10-2 : Cable Assembly Drawing, P&D-D ⇔ Microribbon

10.3.2 Pin Definitions, P&D-D ⇔ Microribbon

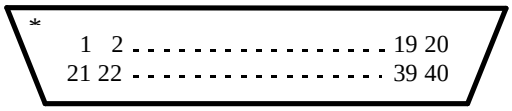
Pin	P&D-D Connector Main Field	Pin	0.050" 40 pin Microribbon Connector
1	TMDS Data2 +	8	TMDS Data2+
2	TMDS Data2 -	7	TMDS Data2-
3	TMDS Data2 return	27	TMDS Data2 return
4	Unused		Not applicable
5	Unused		Not applicable
6	Unused		Not applicable
7	TMDS Clock return	21	TMDS Clock return
8	Charge power +	22, 24	Charge power +
9	1394 pair A, data -	19	1394 pair A, data -
10	1394 pair A, data +	20	1394 pair A, data +
11	TMDS Data1 +	6	TMDS Data1+
12	TMDS Data1 -	5	TMDS Data1-
13	TMDS Data1 return	25	TMDS Data1 return
14	TMDS Clock +	1	TMDS Clock+
15	TMDS Clock -	2	TMDS Clock-
16	USB data +	33	USB data +
17	USB data -	34	USB data -
18	1394 outer shield (optional) & Charge power return	26, 28	Charge power return
		14	USB return
		39	1394 pair A return
		37	1394 pair B return
19	1394 Vg	38, 40	1394 Vg
20	1394 Vp	16, 36	1394 Vp
21	TMDS Data0 +	4	TMDS Data0+
22	TMDS Data0 -	3	TMDS Data0-
23	TMDS Data0 return	23	TMDS Data0 return
24	Unused		Not applicable
25	DDC return	11	DDC return
26	DDC data (SDA)	31	DDC data (SDA)
27	DDC clock (SCL)	12	DDC clock (SCL)
28	+5V dc	15, 35	+5V dc
29	1394 pair B, clock+	17	1394 pair B, clock+
30	1394 pair B, clock -	18	1394 pair B, clock -
		13, 32	+5V dc return

Figure 10-3 : Pin Definitions, P&D-D ⇔ Microribbon

Numbering convention on P&D-D plug:



Numbering Convention on microribbon plug:



* Pin # 1 identification mark

Notes:

1. 1394 shields and Charge power return are bussed at pin 18 of the P&D-D connector, the 1394 pair A shield is connected to pin 39, the 1394 pair B shield is connected to pin 37 and the Charge power return is bussed at pins 26 & 28 of the 40 pin microribbon connector.
2. For 1394 Vg, two wires are connected to pin 19 of the P&D-D connector and connected separately to pins 38 and 40 in the 40 pin ribbon connector in order to safely handle the 1.5A current required by the 1394 specification.

3. For 1394 Vp, two wires are connected to pin 20 of the P&D-D connector and connected separately to pins 16 and 36 in the 40 pin ribbon connector in order to safely handle the 1.5A current required by the 1394 specification.
4. Connector drawings not to scale and looking at plug face.
5. For +5V dc, two wires are connected to pin 28 of the P&D-D- connector and connected separately to pins 15 and 35 in the 40 pin ribbon connector.

11. Appendix B: Software Considerations at Start-Up

This appendix is for information only and is a suggestion on how the operating system may interact with the Plug & Display graphic subsystem. The processes described correspond to the layer of code above the processes described in section 2.3 Hot Plugging.

11.1 Power on Sequences

11.1.1 System Unit Powers on after Monitor Power On

Initialisation
- Prior to System Unit Power on Reset
- The Monitor resets itself to the state as defined in the Monitor Quiescent State
  - Monitor not displaying
  - Channels Disabled
- System Unit provides +5V to DDC
- Monitor leaves Quiescent state
- Monitor Display enabled
- System Unit reads DDC
- Channels enabled as per EDID data

If Command Layer Present
- Then
  - Start Command Layer
  - Hand Control to Command Layer
  - Test for presence of Monitor
  - Monitor response
  - Continue
  - .....

Else
- Start Adapter Layer
- Hand Control to adapter Layer
- Continue
- .....

11.1.2 System Unit Powers on and Monitor Not Powered On

Initialisation
System Unit provides +5V to DDC
Read EDID
If Command Layer Present
Then
Start Command Layer
Hand Control to Command Layer
Test for presence of Monitor
Is Charge Power line >2.0V ?
Continue to test at set time intervals
.....
The Monitor powers on Quiescent State
Monitor not displaying
Channels disabled
Monitor leaves Quiescent State
Monitor Display enabled
Monitor responses
Continue
.....
Else
Start Adapter Layer
Hand Control to adapter Layer
The Monitor resets itself to the state as defined in the Monitor Quiescent State
Is Charge Power line >2.0V ?
Monitor not displaying
All Channels enabled
Monitor leaves Quiescent state
DPMS enables monitor

Continue
.....

11.1.3 System Unit IPL after Monitor Power On

No Vsync., Hsync. Or TMDS activity
The Monitor sets itself to the state as defined in the Monitor Quiescent State
Monitor not displaying
Channels disabled
System Unit starts
.....
.....
System IPL
System Unit reads EDID
Is there Vsync. & Hsync. or syncronised TMDS activity ?
Then
Monitor leaves Quiescent state
Monitor Display enabled
Else

If Command Layer Present
Then
Start Command Layer
Hand Control to Command Layer
Test for presence of Monitor
Monitor response
Continue
.....
Else
Start Adapter Layer
Hand Control to adapter Layer
DPMS moves Monitor out of Power management state
Continue
.....

12. Appendix C: Guidance on Implementation

12.1 P&D Family of Connectors

The VESA Plug and Display Standard (this document) builds on the VESA Enhanced Video Connector Physical Standard (EVC), extending that concept into a family of related connectors which exist under a common logical interface architecture. The original EVC definition fits into this family as the connector standard of choice for systems choosing to support only an analogue video interface. The two new connector standards introduced here complete the family, providing standards for supporting both analogue and digital video interfaces on a single host connector, and for supporting a digital only host. The relationship between these connectors and the corresponding monitor video connectors is shown in following diagram.

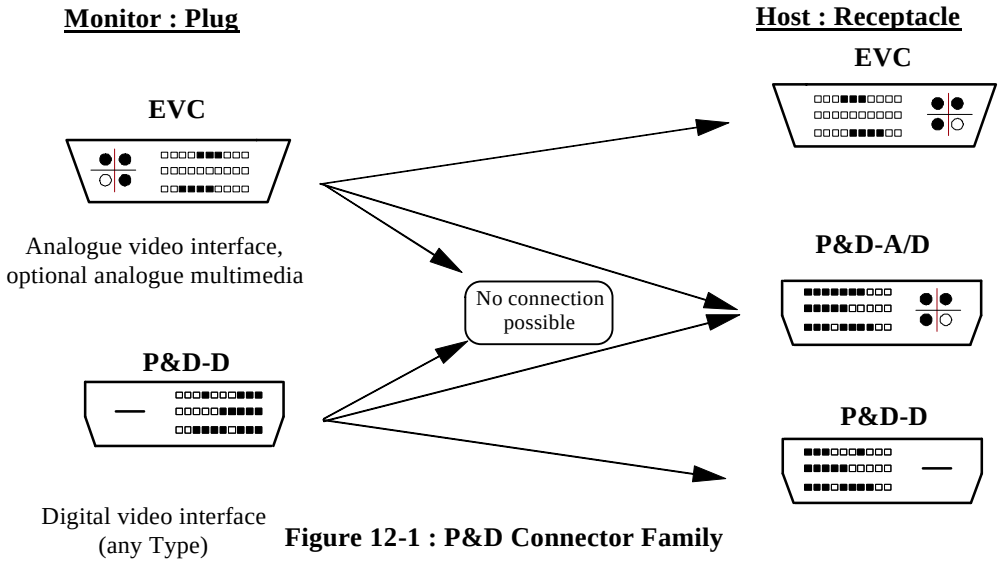


Figure 12-1 : P&D Connector Family

Note: The black pins/sockets above indicate the pins/sockets used in the minimum configuration.

This family of connectors uses a combination of shell shape and other physical features to ensure that displays using a given interface type (either analogue or digital) will not be connected to hosts which do not provide support for that interface, but can always be connected to hosts on which that interface may be supported.

Analogue interface monitors will use the original EVC plug, and so may be supported on both analogue only hosts (with the P&D-A/D receptacle) and on those hosts which provide both analogue and digital support (via the P&D-A/D receptacle).

Digital interface monitors, using a plug which has no provision for analogue connections, are supported on any host which provides a digital output but will not be capable of being connected to hosts supplying only analogue video. Similarly, analogue input monitors cannot be connected to hosts providing support only for digital video.

12.2 Plug - Receptacle Physical Compatibility Summary

	Host Receptacle EVC	Host Receptacle P&D - A/D	Host Receptacle P&D - D
Monitor Plug : EVC	Yes	Yes	No
Monitor Plug : P&D - D	No	Yes	Yes

Figure 12-2 : Plug Receptacle Physical Compatibility

13. Appendix D: Power-Up and Hot-Plugging of P&D Hosts and Monitors

This is an informative appendix and does not form part of the VESA plug and Display Standard.

This appendix is provided to assist in navigating the many subtle details involved in the initial stages of configuring a P&D host to work with an attached monitor. Potential pit-falls are introduced by the probability that P&D hosts and P&D monitors will, on occasion, be attached to non-P&D compliant hardware. Also, it is necessary to try to gracefully handle instances of poorly-made connections between hosts and monitors using extension cables and/or countless conceivable forms of adaptive hardware. Of course, it is not possible to completely "fool-proof" this interface against all possible contingencies.

13.1 Requirements of P&D Hosts

All P&D hosts are required to supply +5.0VDC on the +5V DDC line to the monitor. P&D-D monitors depend on being able to use the presence of this +5V supply as a prerequisite to enabling their TMDS receivers.

In all P&D hosts, a HARDWARE-BASED mechanism should be used to continuously monitor the Charge Power line for the presence of at least +2.0V from the monitor supplied on the Charge Power line, and to do the work of disabling the host's TMDS transmitter whenever that voltage falls below +2.0V. A mechanism requiring the support of software that runs on the host CPU should NEVER be used to perform this function. The intention is that it should be possible for this feature to work even if the host system is "hung."

13.2 Requirements of P&D Monitors

P&D monitors are required to supply a minimum +2.4V output on the Charge Power line to the host. The host makes use of the presence of this power supply in determining whether or not a monitor is attached.

Adaptive hardware designed to allow non-P&D monitors (including older CRT monitors), to be used with hosts that are compliant with the Plug and Display standard must, as a minimum, strap the +5V DDC line originating from the host to the Charge Power line going back to the host. A manufacturer of such adaptive hardware should strive to design such that it is easier to connect and disconnect the display from the host at the host's P&D interface than at the point where the adaptive hardware attaches to the monitor. Doing this will help to ensure that the P&D host is able to receive an indication of whenever the monitor is connected or disconnected.

13.3 Power-Up and Hot-Plugging Sequence of Events for P&D-A/D Host

Figure 13.1 presents a flowchart of the sequence of actions taken by a P&D host upon being turned on or reset. The following paragraphs follow some of the possible sequences of events to support the attachment of various types of monitors.

13.3.1 P&D-D Monitor Attached to P&D-A/D Host

In this scenario, a P&D-D monitor has been attached to a P&D-A/D host, and the host has just been turned on or reset.

The host begins by attempting to read EDID at DDC address A2h, which would be successful, since the monitor is compliant with P&D. By examining the contents of the EDID structure received, the host determines that the TMDS interface will be used. The host then double-checks to see that a voltage level of +2.4V or higher is being received from the monitor on the Charge Power line. Presuming that there are no problems with either the monitor or the cable connecting it to the host, the host will find at least +2.0V to be present and will, therefore, turn on its TMDS transmitter and begin sending an image to the display using the various parameters found within the EDID structure. Normal display operation has begun.

While normal display operation continues, hardware within the host continuously monitors the Charge Power line for any occasion in which the voltage level might drop below +2.0V. Such an event would presumably mean that the display has been disconnected from the host. Should such an event occur, the monitoring hardware in the host would immediately disable the TMDS transmitter. That same monitoring hardware would then continuously monitor the Charge Power line to see if the voltage level ever rises back to +2.0V or higher. Presumably, the return of a voltage level of +2.0V or higher would mean that a display has just been connected to the host. Since it is not prudent to assume that the monitor just connected is necessarily the same one that had been disconnected earlier, the monitoring hardware does NOT re-enable the TMDS transmitter. Instead, the monitoring hardware signals the host via an interrupt (or similar means) that a monitor has just been connected. This signal would cause the host to repeat the earlier process to identify and configure itself for the newly attached display.

13.3.2 EVC Monitor Attached to P&D-A/D Host

In this scenario, an EVC monitor has been attached to the host, and the host has just been turned on or reset.

The host begins by attempting to read EDID at DDC address A2h, which would be successful, since the monitor is compliant with P&D. By examining the contents of the EDID structure received, the host would determine that the analogue interface will be used, and will, therefore, turn on its D-to-A converters and begin sending an image to the display using the various parameters found within the EDID structure. Normal display operation has begun.

While normal display operation continues, hardware within the host continuously monitors the Charge Power line for any occasion in which the voltage level might drop below +2.0V. Such an event would presumably mean that the display has been disconnected from the host. Even when such an event occurs, however, display output through the D-to-A converters would actually continue. Should such an event occur, the same monitoring hardware then continuously monitors the Charge Power line to see if the voltage level ever rises back to +2.0V or higher. Presumably, the return of a voltage level of +2.0V or higher would mean that a display has just been connected to the host. Since it is not prudent to assume that the monitor just connected is necessarily the same one that had been disconnected earlier, the monitoring hardware would immediately disable the D-to-A converters. The monitoring hardware would then signal the host via an interrupt (or similar means) that a monitor has just been connected. This signal would cause the host to repeat the earlier process to identify and configure itself for the newly attached display.

13.3.3 Non-P&D Monitor Attached to P&D-A/D Host

In this scenario, a monitor that uses an analogue interface, and which is not compliant with P&D, has been attached to a P&D-A/D host, and the host has just been turned on or reset.

The host begins by attempting to read EDID at DDC address A2h, which might very well fail, since the monitor is not compliant with P&D. The lack of an EDID structure can be used as the basis of a assumption that the monitor (if one is attached) will be using the analogue interface, and not TMDS. The host then attempts to read an earlier incarnation of EDID at DDC address A0h. If the display has this earlier EDID structure, then the sequence of events would continue with the host using the information in that EDID structure to configure its output as appropriate before turning on its D-to-A converters. Normal display operation would thereby begin.

However, if no EDID structure was found at A0h, the host would be forced to make more assumptions concerning the attached monitor. If the host is a typical personal computer, it may well presume that any monitor attached to it is an older VGA-standard monitor. Such a host would turn on the D-to-A converters and then check the R, G and B analogue output lines to determine if a load exists on all three outputs. If such a load is present, the host would likely assume that it has been attached to a colour VGA monitor. If there is no such load present, then the host would then likely check the G analogue output line to determine if a load exists on it alone. If such a load is present, the host would likely assume that it has been attached to a monochrome VGA monitor. If there is no such load present, then the host would likely assume some other appropriate default form of monitor. Whatever the result, the host would then configure its output as appropriate, and normal display operation would begin.

However, if the host is not a personal computer, but a workstation belonging to a family of workstations with a family of monitors dating from before the introduction of P&D, the host should perform whatever loading tests and make whatever presumptions concerning the resolution and frequency of the attached monitor that would be appropriate for monitors in its product line. Whatever the result, the host would then configure its output as appropriate, and normal display operation would begin.

While normal display operation continues, hardware within the host continuously monitors the Charge Power line for any occasion in which the voltage level might drop below +2.0V. Such an event would presumably mean that the display has been disconnected from the host. However, it is also possible that the non-compliant monitor in this case, or the adaptive hardware used to attach that monitor to the host does not provide a voltage on the Charge Power line. For this reason, display output through the D-to-A converters actually continues even if this voltage is lost, or was simply never provided. In such circumstances, the monitor would be operating in an alternate form of normal operating mode in which the monitoring hardware continuously monitors the Charge Power line to see if the voltage level ever rises back to +2.0V or higher. Presumably, the onset of a voltage level of +2.0V or higher would mean that a display (perhaps one compliant with P&D) has just been connected to the host. Since it is not prudent to assume that the monitor just connected is the same one that had been disconnected earlier, the monitoring hardware would immediately disable the D-to-A converters. The monitoring hardware would then signal the host via an interrupt (or similar means) that a monitor has just been connected. This signal would cause the host to repeat the earlier process to identify and configure itself for the newly attached display.

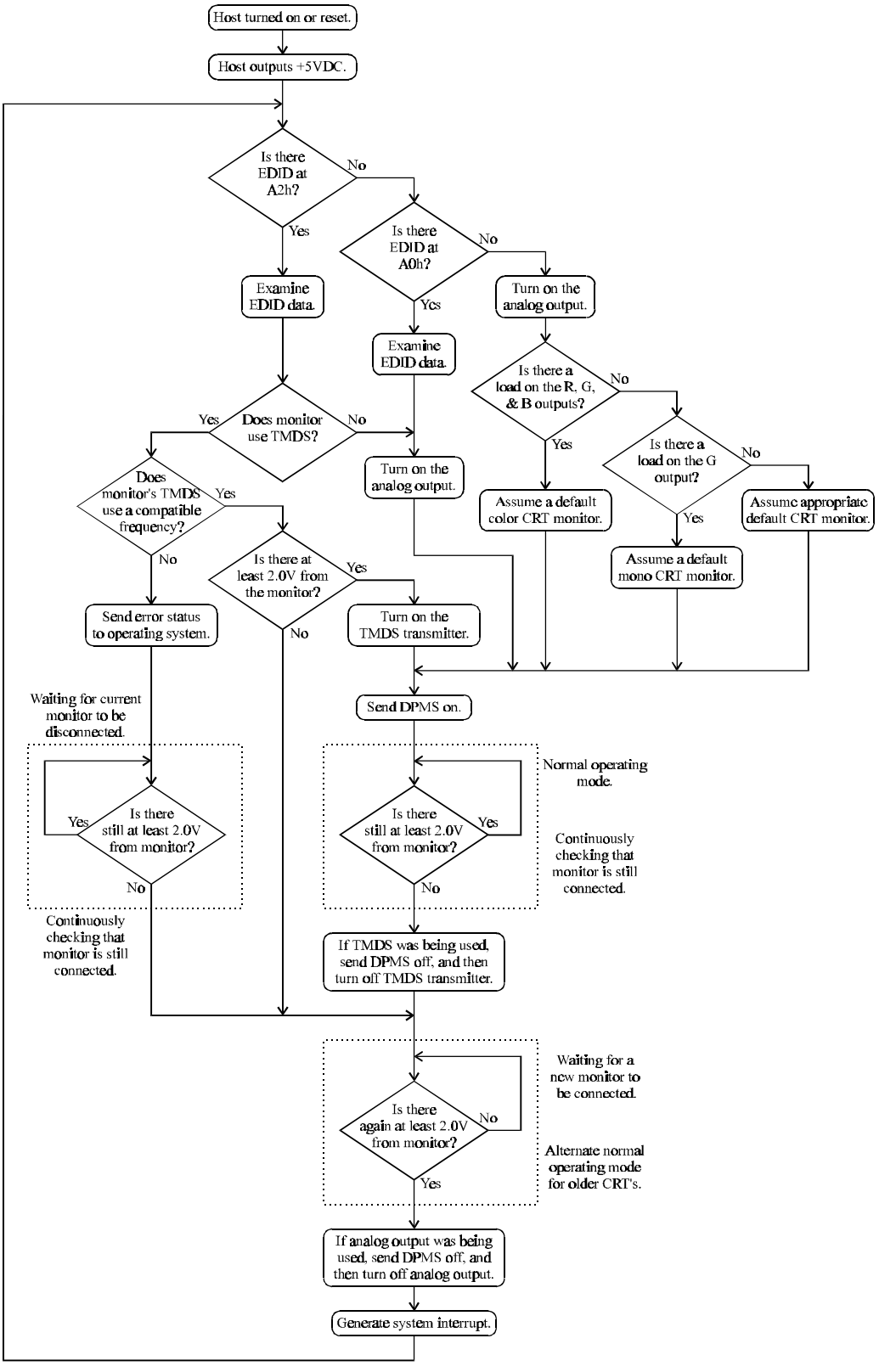


Figure 13-1 : Power-Up and Hot Plugging Flowchart for P&D-A/D Host

13.4 Power-Up and Hot-Plugging Sequence of Events for P&D-D Host

Figure 13.2 presents a flowchart of the sequence of actions taken by a compliant host with only a TMDS output capability upon being turned on or reset. The following paragraphs follow some of the possible sequences of events for various types of monitors.

13.4.1 P&D-D Monitor Attached to P&D-D Host

In this scenario, a P&D-D monitor has been attached to a P&D-D host, and the host has just been turned on or reset.

The host begins by checking that +2.0V or higher is being received from the monitor on the Charge Power line, which would be the case, since the monitor complies with P&D. The host then attempts to read the monitor's EDID at DDC address A2h, and which presumably would succeed. By examining the contents of the EDID structure received, the host determines that the TMDS interface is what the monitor requires. The host then turns on its TMDS transmitter and begins sending an image to the display using the various parameters found within the EDID structure. Normal display operation has begun.

While normal operation continues, hardware within the host continuously monitors the Charge Power line for any occasion in which the voltage level might drop below +2.0V. Such an event would presumably mean that the display has been disconnected from the host. Should this occur, the monitoring hardware in the host would immediately disable the TMDS transmitter. That same monitoring hardware would then continuously monitor the Charge Power line to see if the voltage level ever rises back to +2.0V or higher. Presumably, the return of a voltage level of +2.0V or higher would mean that a display has just been connected to the host. Since it is not prudent to assume that the monitor just connected is necessarily the same one that had been disconnected earlier, the monitoring hardware does NOT re-enable the TMDS transmitter. Instead, the monitoring hardware signals the host via an interrupt (or similar means) that a monitor has just been connected. This signal would cause the host to repeat the earlier process to identify and configure itself for the newly attached display.

13.4.2 Monitor with Analogue Interface Attached to P&D-D Host

Although the physical design of the connectors should not allow this to occur, it is conceivable that through ad-hoc efforts on the part of end-users, or improperly designed adaptive hardware or extension cables, a situation might arise where somehow a monitor requiring analogue input is attached to a P&D-D host.

The host begins by checking to that +2.0V or higher is being received from the monitor on the Charge Power line, which would be the case if the monitor is happens to comply with P&D. The host then attempts to read EDID at DDC address A2h, which presumably would succeed if the monitor happens to comply with P&D. However, either by the absence of either a voltage on the charge power line or an EDID structure at A2h, or by the reading the EDID structure, the host would either assume or discover that it has been attached to a monitor requiring an analogue interface. Since the host is not capable of providing an analogue output, the host would first send an error status message to the operating system, and then it would being continuously monitoring the Charge Power line for any occasion in which the voltage level might drop below +2.0V, indicating that the incompatible display has been disconnected. That same monitoring hardware would then continuously monitor the Charge Power line to see if the voltage level ever rises back to +2.0V or higher. Presumably, the return of a voltage level of +2.0V or higher would mean that a monitor has just been connected to the host. The monitoring hardware then signals the host via an interrupt (or similar means) that a monitor has just been connected. This signal would cause the host to repeat the earlier process to identify and configure itself for the newly attached display.

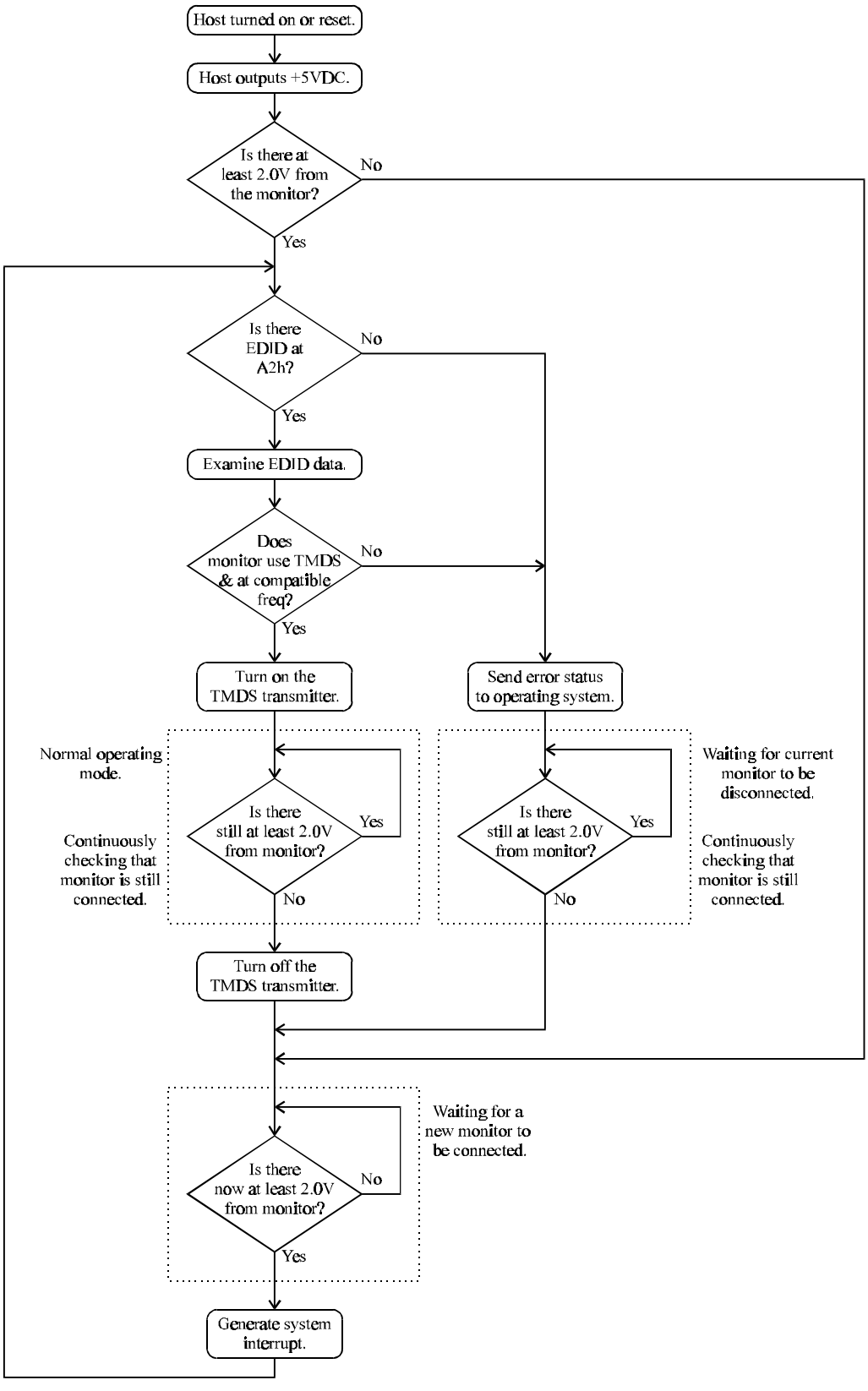


Figure 13-2 : Power-Up and Hot-Plugging Flowchart for P&D-D (TMDS) Host

13.5 Power-Up and Hot-Plugging Sequence of Events for P&D-D Monitor

Figure 13.3 presents a flowchart of the sequence of actions taken by the circuitry of a compliant monitor requiring TMDS input upon being connected to a power source. It is expected that the monitor will default to being essentially in the DPMS off state upon first being connected to a power source.

The monitor would continuously watch the +5V DDC line received from the host for the presence of +5.0V. Presumably, this would mean that the monitor has just been connected to an active compliant host, or that the host has just been turned on. The monitor would also continuously watch for when the host reads all 256 bytes of the monitor's EDID structure at A2h. This would presumably mean that the host is, in fact, compliant with the Plug and Display specification, and that it should now be aware of the monitor's requirements. In response to this reading of the EDID structure, the monitor would turn on its TMDS receiver.

While continuing to check for the presence of +5.0V from the host, the monitor would wait until it starts receiving SHFCLK pulses from the host before powering up its flat panel (presuming this is a flat panel monitor) and entering normal operating mode. If the monitor supports DPMS, then in normal operating mode the monitor would watch the horizontal and vertical sync. signals (or their flat panel equivalents) for indications of which of the four possible DPMS states it should enter.

Throughout normal operation, the monitor would also continuously watch for either the cessation of SHFCLK, or the absence of +5.0V on the +5V DDC line. Should either of these happen, the monitor would power down its flat panel (if it is not already powered down) and disable its TMDS receiver - essentially the equivalent of entering the DPMS off state. The monitor would then go back to waiting for +5.0V to be reestablished and for its EDID structure at A2h to be read again, before re-enabling its TMDS receiver.

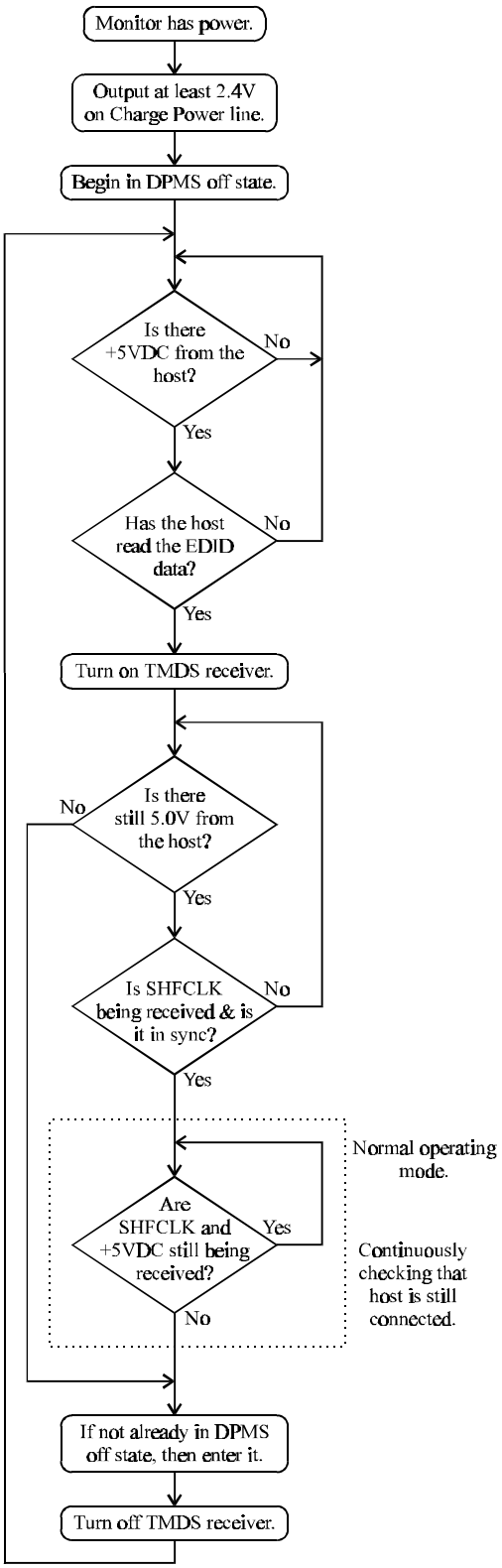


Figure 13-3 : Power-Up and Hot-Plugging Flowchart for P&D-D (TMDS) Monitor

14. Appendix E : Measurement Protocols

14.1 Bandwidth Measurements

14.1.1 Scope and objective

The purpose of this test is to evaluate the bandwidth performance of a connector and/or a connection system. This is necessary to determine the impact of the connection for the system in which it is used.

This measurement is the high frequency half power point (-3dB power point).
The frequency domain procedure used will measure the first order (20dB/decade) half power point (roll off frequency) of the connection. This data can then be used to determine the connection's impact on the system in which it is used.

Once the bandwidth data is known, a complex waveform can be analyzed. The complex waveform (system waveform) can be broken down into its fundamental components and each frequency that passes through the connection can be analyzed. Another approach is to convert the bandwidth (frequency domain) data to time domain information and then analyze the impact the connection will have on the system's waveform.

14.1.2 Test Equipment

The equipment of choice for frequency domain measurements is the Network Analyzer. Bandwidth measurements require a swept frequency source and receiver capable of a flat amplitude response over the frequency range of measurement. The Network Analyzer provides both the swept source and tuned (flat amplitude response) receiver ports necessary for the bandwidth measurement.

A test fixture is needed to attach the device under test (DUT) to the network analyzer's two ports.

14.1.3 Test Specimen

Two connections, to the Device Under Test (DUT), are described. In each case a complete connection must be made which will be an accurate representation of the final connection.

1. Connector (mated two pieces): The connector should be a mated pair with multiple contacts. This connector type has contacts that typically consist of two halves that are mated together to complete the connection. Typical applications are board to board, board to wire, and wire to wire.

2. Connection (connector mated to card edge): The interconnection should be complete, in that the test specimen should not be altered electrically when used in a system. For card edge connectors, the mating card edge or connection must be in place to test the connection.

14.1.4 Test Fixture

The test fixture should provide the interconnect between the network analyzer and the DUT. The test fixture can provide the signal to ground pattern for which the DUT will be tested. If the test fixture does not include the signal to ground pattern connections, it should be part of the DUT. The fixture should provide a controlled impedance setup. The fixture should be as similar to the intended application as possible. This includes cable and/or printed circuit board connections.

14.1.5 Test Method

The network analyzer, test fixture, and DUT should be connected as in Figure 14.1. The DUT should be mounted in the test fixture in a manner that is as close to the actual application of the connector as possible. The test fixture connects to the source and receive ports of the network analyzer.

The network analyzer frequency range can be set to sweep logarithmically over several decades to monitor the first order roll off. The amplitude should be set to monitor in -dB.

The DUT can be measured and the corresponding first order roll off frequency can be monitored at the -3dB point. Filtering should not be used as it can mask the data. However, it can be useful in determining if the -3dB point is the first order roll off frequency.

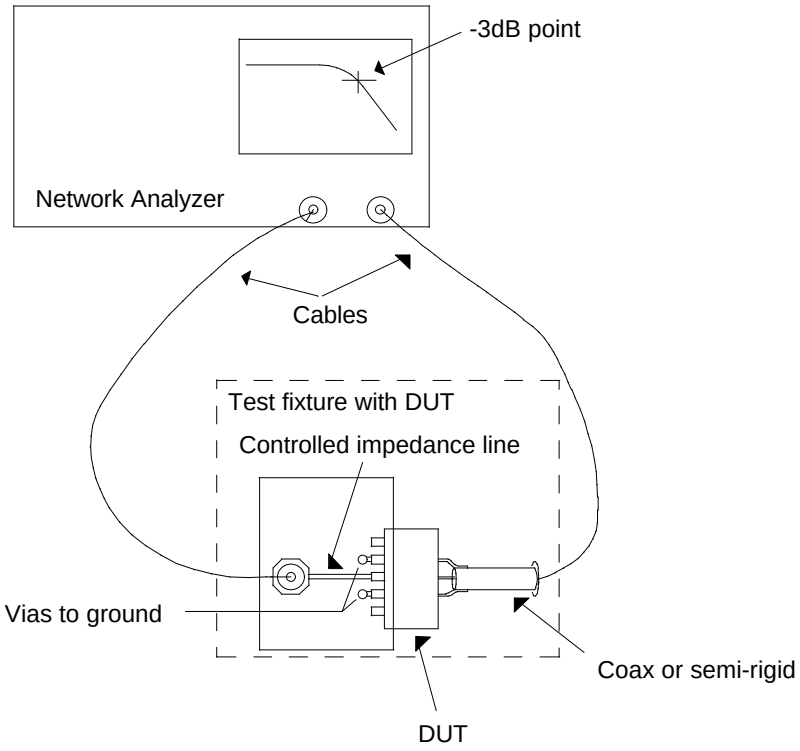


Figure 14-1 : Bandwidth Measurement Set-Up

14.2 Shell-to-Shell and Shell-to-Bulkhead Resistance

14.2.1 Scope & Objectives

This procedure is to be used to determine the shell to shell and/or shell to bulkhead resistance.

Shell to shell resistance is indicative of connector conduction.

Shell to bulkhead resistance is indicative of electrical bonding.

14.2.2 Measurement Equipment

1. Voltmeter
   Capable of measuring the voltage within +/- 2% of the desired value.
2. Ammeter
   Capable of measuring the current within +/- 1% of desired value.
3. Regulated Power
   Supply Capable of delivering 1.0A +/- 0.1A
4. Test Probes
   Spherical ends of 1.27mm (0.50 inch) minimum radius shall be used to make contact on the connector and mounting surfaces.

14.2.3 Test Specimen

The test shall consist of a mated connector (plug + receptacle) or receptacle mounted to a conductive surface (bulkhead). Test specimen shall be wired or unwired as specified in the Detail Specification.

When assessing shell to shell resistance the mated connectors shall be placed on a non-conductive surface.

14.2.4 Test Procedure

Unless otherwise specified, a current of 1.0A +/- 0.1A dc at 1.5 volts maximum shall be passed through the mated connector or through the receptacle and the mounting surface (bulkhead).

14.2.5 Shell to Shell Resistance

Unless otherwise specified, the voltage drop across the mated connector shall be measured from a point on the rear accessory thread of the plug to the mounting flange on the receptacle. On square flange receptacles, the point of measurement shall be adjacent to the mounting hole.

14.2.6 Receptacle to Bulkhead Resistance

Unless otherwise specified, the voltage drop across the receptacle mounted to the bulkhead shall be measured from a point on the rear of the accessory thread on the plug to a point on the bulkhead next to the mounting flange. Be careful that the probe does not touch the mounting flange.

14.2.7 Details to be Specified

The following details shall be specified in the Detail Specification:

1. Number of samples to be tested.
2. Test current if other than specified herein.
3. Point(s) of measurement if other than specified herein.
4. Voltage drop

14.2.8 Test Documentation

Documentation shall contain the following:

1. Title of test
2. Description of specimen (and fixture, if applicable)
3. Test equipment used and date(s) of last calibration
4. Values and observations
5. Ambient temperature and humidity (as applicable)
6. Point(s) of voltage measurement
7. Details of receptacle mounting (if applicable)
8. Name of operator and test date